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10015055-1

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Daniel J. Dove
Serial No.:	09/939,418
Conf. No.:	4205
Filed:	08/24/2001
For:	REDUCED PIN-COUNT SYSTEM INTERFACE FOR GIGABIT ETHERNET PHYSICAL LAYER DEVICES
Art Unit:	2665
Examiner:	Khuong, Lee T.

I hereby certify that this paper is being deposited with the United States Postal Service as FIRST-CLASS mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this date.

12/6/05

Date Registration No. 28124

F-CLASS.WCM

Appr. February 20, 1998 *Attorney for Applicant(s)*

DECLARATION OF DANIEL J. DOVE OF PRIOR INVENTION TO OVERCOME CITED PUBLICATION (37 C.F.R. §1.131)

1. I am the named inventor of the claimed subject matter of the above-identified patent application.

2. I have reviewed the Lo 6,920,132 patent that has been cited by the examiner in the above-identified patent application. The Lo patent is indicated to be assigned to Marvel International Ltd.

3. The above-referenced patent application was filed after I invented a reduced gigabit media independent interface. In connection with the development of this interface, I contacted several companies in an effort to reach agreement on design features and functionality that would be used by Hewlett-Packard and other companies and become a defacto industry standard. I conceived the invention prior to the date of June 29, 1999 which is the date of the document entitled "Reduced Gigabit Media Independent Interface (RGMII), Revision 1.2, that is attached hereto as Exhibit

1., which predates Lo 6,920,132 patent filing date of May 30, 2000. I also ran extensive computer simulations of the circuit design which confirmed the operability of the circuit design. Such simulations are common practice for design engineers and are extremely reliable demonstrators of the adequacy and operability of particular designs of integrated circuits as is known to those of ordinary skill in integrated circuit design and development.

4. I disclosed my invention to Marvel under a confidential disclosure agreement (CDA) such as the CDA shown in attached Exhibit 2 that has an effective date of September 28, 1999, and which was signed by National Semiconductor. Other companies which were provided similar information included Agilent, Broadcom and Intel.

5. I prepared the document entitled "Reduced Gigabit Media Independent Interface (RGMII) dated June 29, 1999, Revision 1.2, (Exhibit 1). This document shows the system diagram as well as the signal definitions on page 2, as well as the electrical characteristics, together with a waveform that illustrates multiplexing of data and control information on page 3. This document essentially describes the subject matter of the above-identified patent application.

6. It is noted that the bottom of Exhibit 1 indicates that it was disclosed to National Semiconductor per CDA and it carries the date of 10/27/05. This indicated date is actually the date that this document was printed from an electronic file rather than the date that it was disclosed to National Semiconductor per a CDA. This is because the document was printed from a Word file that had a date code of the type which automatically updates and prints the current date at the time of

printing. The correct date of this document is the date June 29, 1999 which has not changed since it was created.

7. As a result of continued refinement of the interface, I prepared the document having the same title dated 4/3/2000 and indicating a Revision 1.3 attached as Exhibit 3. There is a revision box at the bottom of the title page which describes the revision description as well as the date of the revision. .

7. Additional revisions were made as a result of continuing refinement of the interface, including Revision 1.4 dated May 11, 2000, attached as Exhibit 4, and Revision 1.5, dated May 19, 2000, attached as Exhibit 5.

8. Exhibits 1 and 3 through 5 carry the indication that they are ***revisions***. I used the term "revision" when the document was still a private document that was confidential within the company, and was not shown to anyone without the protection of a nondisclosure agreement. After receiving comments and other feedback on the issues that the recipient companies had with the interface, it was revised and identified as being a *revision* until it became a more public document.

9. On June 1, 2000, the document attached as Exhibit 6 was stated to be released for public review and comment and given the designation ***Version 1.0*** rather than a revision number. As the interface was further refined, it underwent additional versions including Version 1.1 dated August 1, 2000 attached as Exhibit 7, Version 1.1-B' also dated August 1, 2000 attached as Exhibit attached as Exhibit 9, Version 1.2 dated August 10, 2000, attached as Exhibit 10, Version 1.2 dated September 11, 2000 attached as Exhibit 11, Version 1.2A dated September 22, 2000

attached as Exhibit 12, and Version 1.3 dated December 10, 2000 attached as Exhibit

13, and Version 2.0 dated April 1, 2002 that is attached as Exhibit 14.

10. While it was identified as having been "released for public review" on June 1, 2000, it was not actually released at that time. It was released pursuant to a request made by an email from me to Stan Takata, sent June 10, 2002, which is attached as Exhibit 15. The publication was made by adding the above referenced documents (Exhibits 13 and 14) to the technology library at http://www.hp.com/rnd/library/technology.htm which is described on attached "ticket" identified as Exhibit 16, which indicates that it was targeted to be published on 6/19/2002.

11. During the course of refining the interface, William Lo of Marvel Semiconductor sent me proposed changes to the interface on July 25, 2000 which are described in the attached Exhibit 8.

12. As a person signing below, I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under 18 U.S.C. §1001, and that such willful statements may jeopardize the validity of this application or any patent issued thereon.

Dated: 12/05/05

Daniel J. Dove

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Reduced Gigabit Media Independent Interface (RGMII)

6/29/99
Revision 1.2

Reduced Pin-count Interface

For

Gigabit Ethernet Physical Layer Devices

Revision 1.2

HEWLETT® PACKARD

1.0 Purpose

The RGMII is intended to be an alternative to both the IEEE802.3z GMII and the TBI. The principle objective is to reduce the number of pins required to interconnect the MAC and the PHY from a maximum of 28 pins (TBI) to 13 pins. In order to accomplish this objective, the data paths and all associated control signals will be reduced and control signals will be multiplexed together and both edges of the 125MHz clock will be used.

2.0 System Diagram

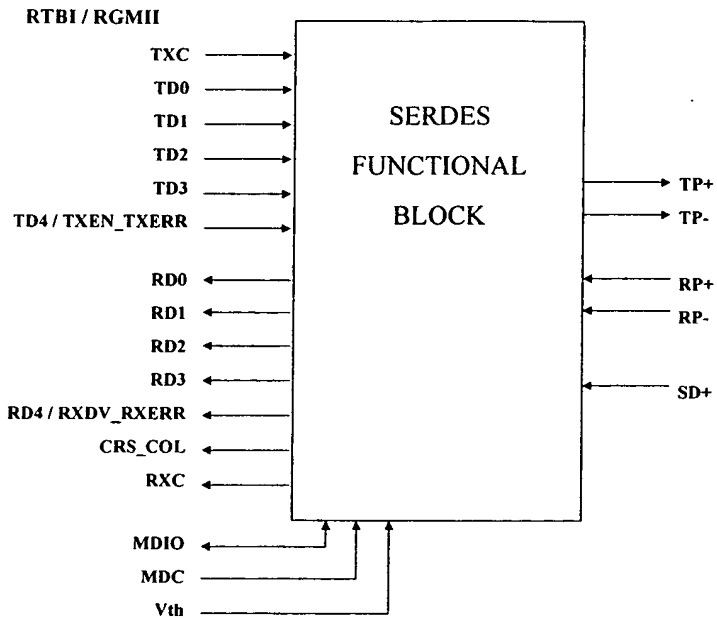

FIGURE 1 (System Diagram)

3.0 Signal Definitions

The RGMII will share four data path signals with the Reduced Ten Bit Interface (RTBI) and share control functionality with the fifth data signal. With the inclusion of the MDIO/MDC serial management signals, the RTBI will not require independent control signals like LK_REF, BYTE_EN, etc.

Signal Name	RTBI	RGMII	Description
TXC	MAC	MAC	The transmit reference clock will be 125Mhz, +-50ppm with a maximum pk-pk jitter of 100ps.
TD[3:0]	PCS	MAC	Contains the lower 4 bits of data on ↑ of TXC, bits 9:6 of the data on ↓ of TXC.
TD[4] TXEN_TXERR	PCS	MAC	In RTBI mode, contains the fifth bit on ↑ of TXC and tenth bit on ↓ of TXC. In RGMII mode, TXEN on ↑ of TXC, TXERR on ↓ of TXC
RXC	PHY	PHY	The receive reference clock will be 125Mhz, +-50ppm. (May be derived from TXC)
RD[3:0]	PHY	PHY	Contains the lower 4 bits of data on ↑ of RXC, bits 9:6 of the data on ↓ of RXC.
RD[4] RXDV_RXERR	PHY	PHY	In RTBI mode, contains the fifth bit on ↑ of RXC and tenth bit on ↓ of RXC. In RGMII mode, RXDV on ↑ of TXC, RXERR on ↓ of TXC
CRS_COL	N/A	PHY (OPT*)	CRS on ↑ of TXC, COL on ↓ of TXC

* CRS_COL required for half-duplex implementations only

TABLE 1

3.1 Electrical Characteristics

The RGMII and RTBI signals will be based upon electrical relationship to a single threshold voltage rather than absolute voltages. By using this approach, the interface will be portable to smaller IC geometry processes.

Parameter	Min	Max	Units
Voh	Vth+.5	2.5	V
Vol	0	Vth-.5	V
Vih	Vth+.2	2.5	V
Vil	0	Vth-.2	V
Vth	.75	1.25	V

TABLE 2

3.2 Multiplexing of Data and Control

Multiplexing of data and control information is done by taking advantage of both edges of the reference clocks, then sending the lower 4 bits on the ↑ edge and the upper 4 bits on the ↓ edge. Control signals can be multiplexed into a single 125MHz clock cycle using the same technique.

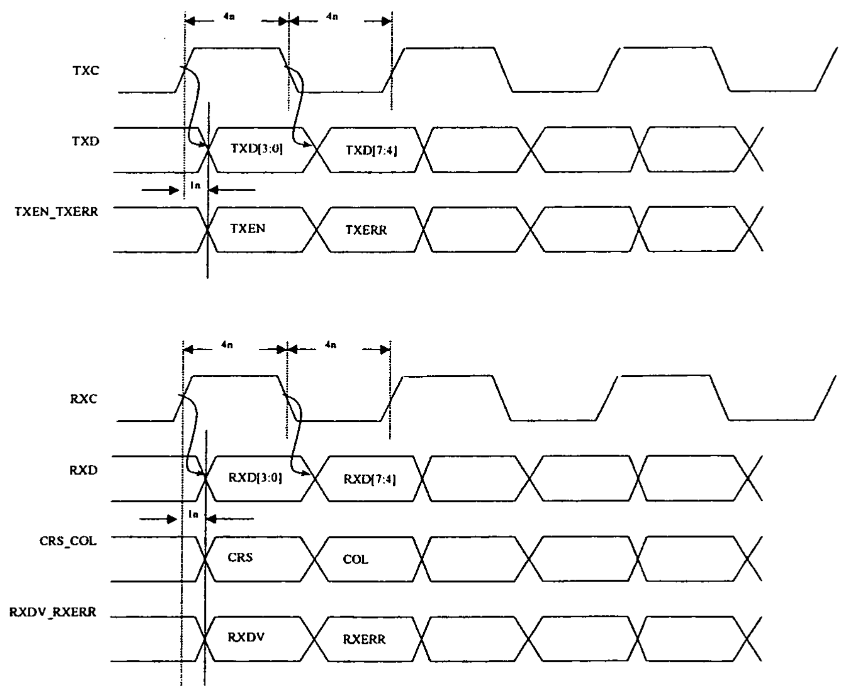

FIGURE 2

3.3 SMII Functionality

This interface can be used to implement the 10/100 Mbps Ethernet Serial Media Independent Interface (SMII) by using TXC, TXD, RXD signals at the 125MHz rate as specified in the SMII ver1.2 document and the SYNCH bit can be multiplexed upon the TXEN signal.

3.4 Mode Selection

The decision about which mode of operation this interface will use is left to the implementer. It may be done with hard-wired pins, or through register bits that are controlled by software.

HEWLETT PACKARD

CONFIDENTIAL DISCLOSURE AGREEMENT

Effective Date: <u>September 28, 1999</u>

In order to protect certain confidential information, Hewlett-Packard Company and it's affiliates (HP), and the Participant identified below, agree that:

1. <u>Disclosing Party:</u> The party disclosing confidential information (Discloser)

is: **<u>Hewlett-Packard Company</u>**
(Note: Fill in HP, Participant, or Both Parties).

2. <u>Primary Representative:</u> Each party's representative for coordinating disclosure or receipt of confidential information is:

HP: **<u>Barbra Stuter</u>**
Participant: **<u>Bill Hagerstrand</u>**

3. <u>Description of Confidential Information:</u> The confidential information disclosed under this Agreement is described as:

HP: **<u>Technical requirements and specifications regarding Reduced Gigabit Media Independent Interface, RGMII</u>**

Participant:

4. <u>Use of Confidential Information:</u> The party receiving confidential information (Recipient) shall make use of the confidential information only for the following purpose (e.g., evaluation and testing for a make/buy decision on project xyz)

HP:
Participant: **<u>Evaluating preparation of proposals for development of new products with this RGMII interface with feature inputs from HP</u>**

5. <u>Confidentiality Period:</u> This Agreement and Recipient's duty to hold confidential information in confidence expire on:

(Note: This is the period of protection of confidential information)

6. Disclosure Period: This Agreement pertains to confidential information that is disclosed between the effective date and:
<u>January 28, 2000</u>
(This is the period during which confidential information is to be disclosed)

7. Standard of Care: Recipient shall protect the disclosed confidential information by using the same degree of care, but no less than a reasonable degree of care, to prevent the unauthorized use, dissemination, or publication of the confidential information as Recipient uses to protect it's own confidential information of a like nature.

8. Marking: Recipient's obligations shall only extend to confidential information that is described in paragraph 3, and that: (a) compromises specific materials individually listed in paragraph 3; or, (b) is marked as confidential at the time of disclosure; or, (c) is unmarked (e.g. orally disclosed) but treated as confidential at the time of disclosure, and is designated as confidential in a written memorandum sent to Recipient's primary representative within thirty days of disclosure, summarizing the confidential information sufficiently for identification.

9. <u>Exclusions:</u> This Agreement imposes no obligation upon Recipient with respect to information that (a) was in Recipient's possession before receipt from Discloser; (b) is or becomes matter of public knowledge through no fault of Recipient; (c) is rightfully received by Recipient from a third party without a duty of confidentiality; (d) is disclosed by Discloser to a third party without a duty of confidentiality on the third party; (e) is independently developed by Recipient; (f) is disclosed under operation of law or; (g) is disclosed by Recipient with Discloser's prior written approval.

10. <u>Warranty:</u> Each Discloser warrants that it has the right to make the disclosures under this Agreement. NO OTHER WARRANTEES ARE MADE BY EITHER PARTY UNDER THIS AGREEMENT. ANY INFORMATION EXCHANGED UNDER THIS AGREEMENT IS PROVIDED "AS IS".

11. <u>Rights:</u> Neither party acquires any intellectual property rights under this Agreement except the limited rights necessary to carry out the purposes set forth in paragraph 4. This Agreement shall not restrict reassignment of Recipient's employees.

<u>Miscellaneous</u>

12. This Agreement imposes no obligation on either party to purchase, sell, license, transfer or otherwise dispose of any technology, services or products.

13. Both parties shall adhere to all applicable laws, regulations and rules relating to the export of technical data, and shall not export or re-export any technical data, any products received from Discloser, or, the direct product of such technical data to any prescribed country listed in such applicable laws, regulations and rules unless properly authorized.

14. This Agreement does not create any agency or partnership relationship.

15. All additions or modifications to this Agreement must be made in writing and must be signed by both parties.

16. This Agreement is made under, and shall be construed according to, the laws of the State of California, USA.

Hewlett-Packard Company

WND/NPSD
8000 Foothills Blvd.
Roseville, Ca 95747-5562

By:______________________________ Date:__________
(Functional Manager's Signature)

____
(Name)

____
(Title)

National Semiconductor
1090 Kifer Road
Mail Stop 16-280
Sunnyvale, CA 94086

By:______________________________ Date:__________
(Authorized Signature)

____
(Name)

____
(Title)

Exhibit 2

Reduced Gigabit Media Independent Interface (RGMII)

4/3/2000
Revision 1.3

Reduced Pin-count Interface
For
Gigabit Ethernet Physical Layer Devices

Revision Level	Date	Revision Description
1.3	**April 3, 2000**	**Changed Interface voltages to HSTL-1 and referenced the EIA/JESD8-6 specification to ease implementation.** **Modified Figure 2 to be consistent with wording in Table 1.**

Exhibit 3

1.0 Purpose

The RGMII is intended to be an alternative to both the IEEE802.3z GMII and the TBI. The principle objective is to reduce the number of pins required to interconnect the MAC and the PHY from a maximum of 28 pins (TBI) to 13 pins in a cost effective and technology independent manner. In order to accomplish this objective, the data paths and all associated control signals will be reduced and control signals will be multiplexed together and both edges of the 125MHz clock will be used.

2.0 System Diagram

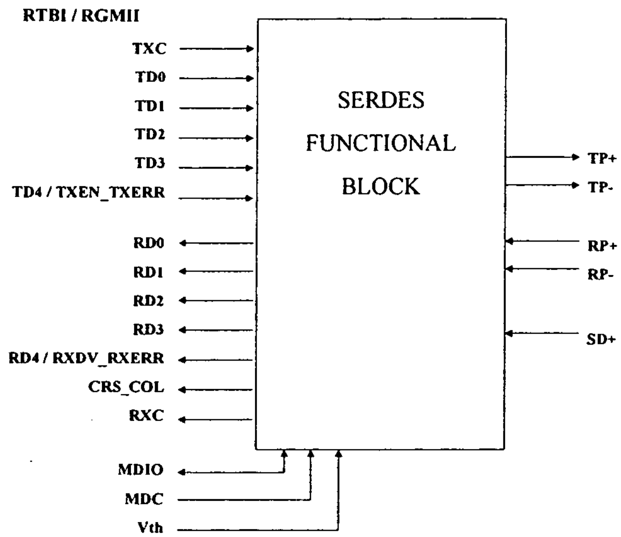

FIGURE 1 (System Diagram)

3.0 Signal Definitions

The RGMII will share four data path signals with the Reduced Ten Bit Interface (RTBI) and share control functionality with the fifth data signal. With the inclusion of the MDIO/MDC serial management signals, the RTBI will not require independent control signals like LK_REF, BYTE_EN, etc.

Signal Name	RTBI	RGMII	Description
TXC	**MAC**	**MAC**	The transmit reference clock will be 125Mhz, +-50ppm with a maximum pk-pk jitter of 100ps.
TD[3:0]	**PCS**	**MAC**	In RTBI mode, contains bits 3:0 on ↑ of TXC and bits 8:5 on ↓ of TXC. In RGMII mode, bits 3:0 on ↑ of TXC, bits7:4 on ↓ of TXC
TD[4]_TD[9] TXEN_TXERR	**PCS**	**MAC**	In RTBI mode, contains the fifth bit on ↑ of TXC and tenth bit on ↓ of TXC. In RGMII mode, TXEN on ↑ of TXC, TXERR on ↓ of TXC
RXC	**PHY**	**PHY**	The receive reference clock will be 125Mhz, +-50ppm. (May be derived from TXC)
RD[3:0]	**PHY**	**PHY**	In RTBI mode, contains bits 3:0 on ↑ of RXC and bits 8:5 on ↓ of RXC. In RGMII mode, bits 3:0 on ↑ of RXC, bits7:4 on ↓ of RXC
RD[4] _RD[9] RXDV_RXERR	**PHY**	**PHY**	In RTBI mode, contains the fifth bit on ↑ of RXC and tenth bit on ↓ of RXC. In RGMII mode, RXDV on ↑ of TXC, RXERR on ↓ of TXC
CRS_COL	N/A	**PHY (OPT*)**	CRS on ↑ of TXC, COL on ↓ of TXC

* CRS_COL required for half-duplex implementations only

TABLE 1

3.1 Electrical Characteristics

The RGMII and RTBI signals will be based upon electrical relationship to a single threshold voltage rather than absolute voltages. By using this approach, the interface will be portable to smaller IC geometry processes. To ease standardization of this interface, HSTL class I signaling is proposed, based upon the EIA/JESD8-6 specification.

Parameter	Min	Typ	Max	Units
VDDO	1.4	1.5	1.6	V
VREF	.68	.75	.90	V
Vih	VREF + .1		VDDO + .3	V
Vil	-.3		VREF - .1	V
Voh	VDDO - .4			V
Vol			.4	V

TABLE 2

3.2 Multiplexing of Data and Control

Multiplexing of data and control information is done by taking advantage of both edges of the reference clocks, then sending the lower 4 bits on the ↑ edge and the upper 4 bits on the ↓ edge. Control signals can be multiplexed into a single 125MHz clock cycle using the same technique.

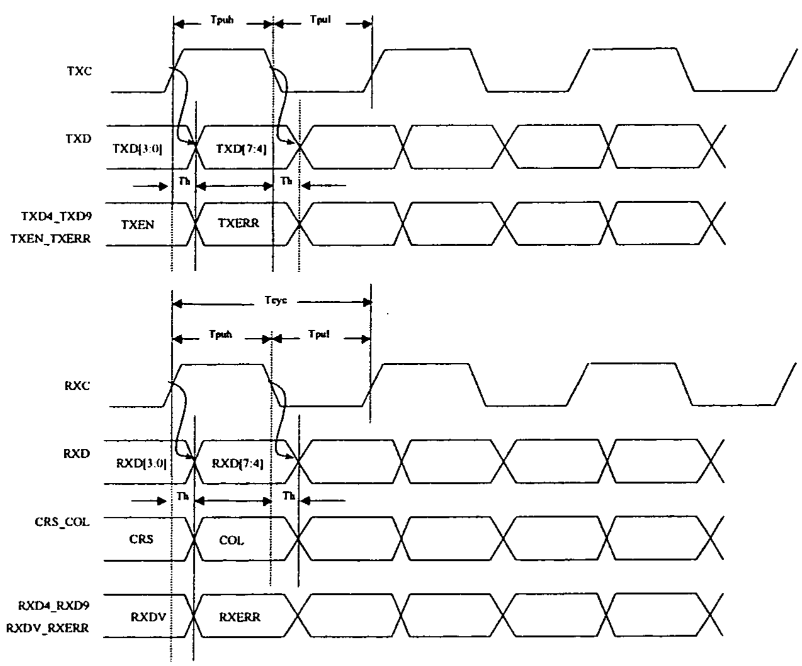

FIGURE 2

3.3 Timing Specifics

Parameter	Min	Typ	Max	Units
Tsu	1	1.5	2	ns
Thold	1		2	ns
Tcyc	7.5	8	8.5	ns
Tpuh	3.5	4	4.5	ns
Tpul	3.5	4	4.5	ns

TABLE 3

3.4 SMII Functionality

This interface can be used to implement the 10/100 Mbps Ethernet Serial Media Independent Interface (SMII) by using TXC, TXD, RXD signals at the 125MHz rate as specified in the SMII ver1.2 document and the SYNCH bit can be multiplexed upon the TXEN signal.

3.5 Mode Selection

The decision about which mode of operation this interface will use is left to the implementer. It may be done with hard-wired pins, or through register bits that are controlled by software.

i n v e n t

Reduced Gigabit Media Independent Interface (RGMII)

5/11/2000
Revision 1.4

Reduced Pin-count Interface
For
Gigabit Ethernet Physical Layer Devices

Revision Level	Date	Revision Description
1.3	**April 3, 2000**	**Changed Interface voltages to HSTL-1 and referenced the EIA/JESD8-6 specification to ease implementation.** **Modified Figure 2 to be consistent with wording in Table 1.**
1.4	**May 11,2000**	**Changed Interface voltages to LVCMOS levels to ease implementation among industry members. This still allows HSTL-1 to be used with a VDDRQ of 2.5v and Vref of 1.25v. Cleaned up timing specs.**

Exhibit 4

1.0 Purpose

The RGMII is intended to be an alternative to both the IEEE802.3z GMII and the TBI. The principle objective is to reduce the number of pins required to interconnect the MAC and the PHY from a maximum of 28 pins (TBI) to 13 pins in a cost effective and technology independent manner. In order to accomplish this objective, the data paths and all associated control signals will be reduced and control signals will be multiplexed together and both edges of the 125MHz clock will be used.

2.0 System Diagram

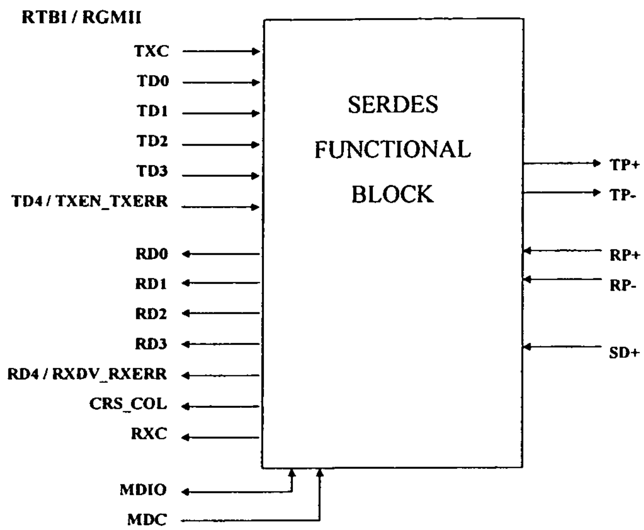

FIGURE 1 (System Diagram)

3.0 Signal Definitions

The RGMII will share four data path signals with the Reduced Ten Bit Interface (RTBI) and share control functionality with the fifth data signal. With the inclusion of the MDIO/MDC serial management signals, the RTBI will not require independent control signals like LK_REF, BYTE_EN, etc.

Signal Name	RTBI	RGMII	Description
TXC	MAC	MAC	The transmit reference clock will be 125Mhz, +-50ppm with a maximum pk-pk jitter of 100ps.
TD[3:0]	PCS	MAC	In RTBI mode, contains bits 3:0 on ↑ of TXC and bits 8:5 on ↓ of TXC. In RGMII mode, bits 3:0 on ↑ of TXC, bits7:4 on ↓ of TXC
TD[4]_TD[9] TXEN_TXERR	PCS	MAC	In RTBI mode, contains the fifth bit on ↑ of TXC and tenth bit on ↓ of TXC. In RGMII mode, TXEN on ↑ of TXC, TXERR on ↓ of TXC
RXC	PHY	PHY	The receive reference clock will be 125Mhz, +-50ppm. (May be derived from TXC)
RD[3:0]	PHY	PHY	In RTBI mode, contains bits 3:0 on ↑ of RXC and bits 8:5 on ↓ of RXC. In RGMII mode, bits 3:0 on ↑ of RXC, bits7:4 on ↓ of RXC
RD[4] _RD[9] RXDV_RXERR	PHY	PHY	In RTBI mode, contains the fifth bit on ↑ of RXC and tenth bit on ↓ of RXC. In RGMII mode, RXDV on ↑ of TXC, RXERR on ↓ of TXC
CRS_COL	N/A	PHY (OPT*)	CRS on ↑ of TXC, COL on ↓ of TXC

* CRS_COL required for half-duplex implementations only

TABLE 1

3.1 Electrical Characteristics

The RGMII and RTBI signals will be based upon 2.5v CMOS interface voltages.

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -1.0mA; V_{CC} = Min	2.1	-	V
V_{OL}	Output Low Voltage	I_{OL} = 1.0mA; V_{CC}=Min	GND	0.40	V
V_{IH}	Input High Voltage		1.7	–	V
V_{IL}	Input Low Voltage		-	.70	V
I_{IH}	Input High Current	V_{CC} = Max; V_{IN} = 2.5V	-	40	μA
I_{IL}	Input Low Current	V_{CC} = Max; V_{IN} = 0.4V	-600	-	μA

TABLE 2

3.2 Multiplexing of Data and Control

Multiplexing of data and control information is done by taking advantage of both edges of the reference clocks, then sending the lower 4 bits on the ↑ edge and the upper 4 bits on the ↓ edge. Control signals can be multiplexed into a single 125MHz clock cycle using the same technique.

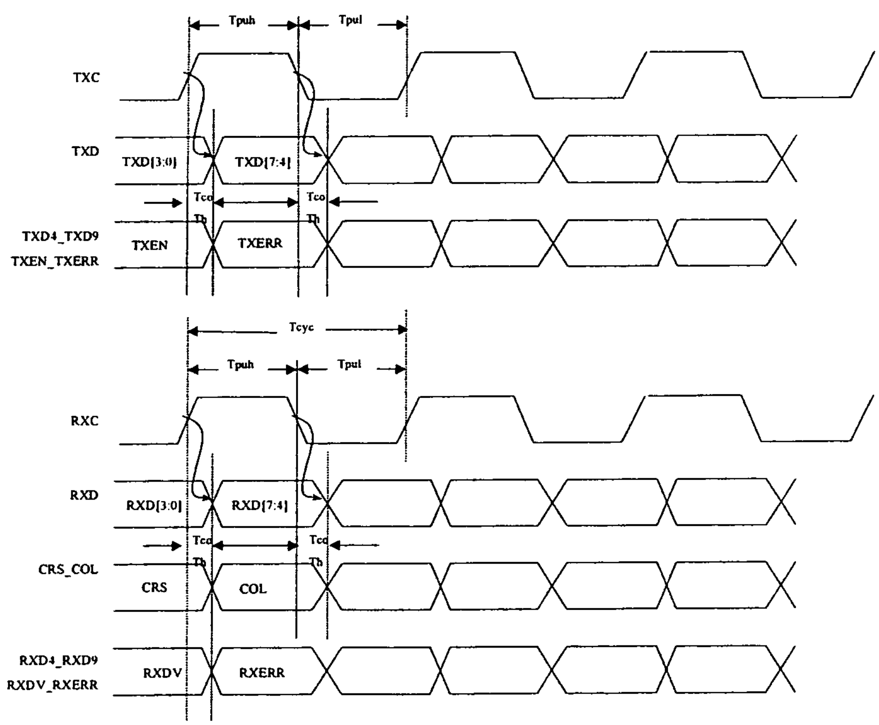

FIGURE 2

3.3 Timing Specifics (Measured with a 20pF / 1KΩ shunt load)

Symbol	Parameter	Min	Typical	Max	Units
Tsu	Setup Time (at Receiver)	1.5			ns
Tco	Clock to Output Delay (at Transmitter)	.5		1.5	ns
Thold	Hold Time (at Receiver)	0			ns
Tcyc	Clock Cycle Duration	7.5	8	8.5	ns
Tpuh	Positive Pulse Width	3.8	4	4.2	ns
Tpul	Negative Pulse Width	3.8	4	4.2	ns
Tr / Tf	Rise / Fall Time (20-80%)			.75	ns

TABLE 3

3.4 SMII Functionality

This interface can be used to implement the 10/100 Mbps Ethernet Serial Media Independent Interface (SMII) by using TXC, TXD, RXD signals at the 125MHz rate as specified in the SMII ver1.2 document and the SYNCH bit can be multiplexed upon the TXEN signal.

3.5 Mode Selection

The decision about which mode of operation this interface will use is left to the implementers. It may be done with hard-wired pins, or through register bits that are controlled by software.

invent

Reduced Gigabit Media Independent Interface (RGMII)

5/19/2000
Revision 1.5

Reduced Pin-count Interface
For
Gigabit Ethernet Physical Layer Devices

Revision Level	Date	Revision Description
1.3	**April 3, 2000**	**Changed Interface voltages to HSTL-1 and referenced the EIA/JESD8-6 specification to ease implementation.** **Modified Figure 2 to be consistent with wording in Table 1.**
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1.5	**May 19, 2000**	**Added Section 3.6 statement regarding Intellectual Property**

Exhibit 5

1.0 Purpose

The RGMII is intended to be an alternative to both the IEEE802.3z GMII and the TBI. The principle objective is to reduce the number of pins required to interconnect the MAC and the PHY from a maximum of 28 pins (TBI) to 13 pins in a cost effective and technology independent manner. In order to accomplish this objective, the data paths and all associated control signals will be reduced and control signals will be multiplexed together and both edges of the 125MHz clock will be used.

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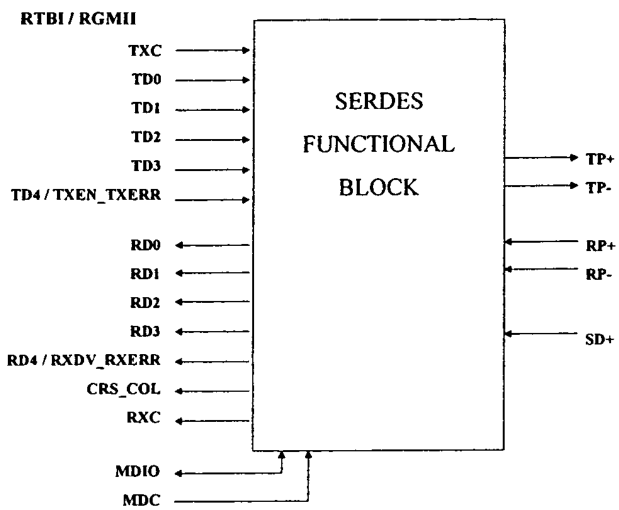

FIGURE 1 (System Diagram)

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TD[3:0]	PCS	MAC	In RTBI mode, contains bits 3:0 on ↑ of TXC and bits 8:5 on ↓ of TXC. In RGMII mode, bits 3:0 on ↑ of TXC, bits7:4 on ↓ of TXC
TD[4]_TD[9] TXEN_TXERR	PCS	MAC	In RTBI mode, contains the fifth bit on ↑ of TXC and tenth bit on ↓ of TXC. In RGMII mode, TXEN on ↑ of TXC, TXERR on ↓ of TXC
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RD[4] _RD[9] RXDV_RXERR	PHY	PHY	In RTBI mode, contains the fifth bit on ↑ of RXC and tenth bit on ↓ of RXC. In RGMII mode, RXDV on ↑ of TXC, RXERR on ↓ of TXC
CRS_COL	N/A	PHY (OPT*)	CRS on ↑ of TXC, COL on ↓ of TXC

* CRS_COL required for half-duplex implementations only

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3.1 Electrical Characteristics

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Symbol	Parameter	Conditions	Min	Max	Units
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V_{OL}	Output Low Voltage	I_{OL} = 1.0mA; V_{CC}=Min	GND	0.40	V
V_{IH}	Input High Voltage		1.7	–	V
V_{IL}	Input Low Voltage		-	.70	V
I_{IH}	Input High Current	V_{CC} = Max; V_{IN} = 2.5V	-	40	ìA
I_{IL}	Input Low Current	V_{CC} = Max; V_{IN} = 0.4V	-600	-	ìA

TABLE 2

3.2 Multiplexing of Data and Control

Multiplexing of data and control information is done by taking advantage of both edges of the reference clocks, then sending the lower 4 bits on the ↑ edge and the upper 4 bits on the ↓ edge. Control signals can be multiplexed into a single 125MHz clock cycle using the same technique.

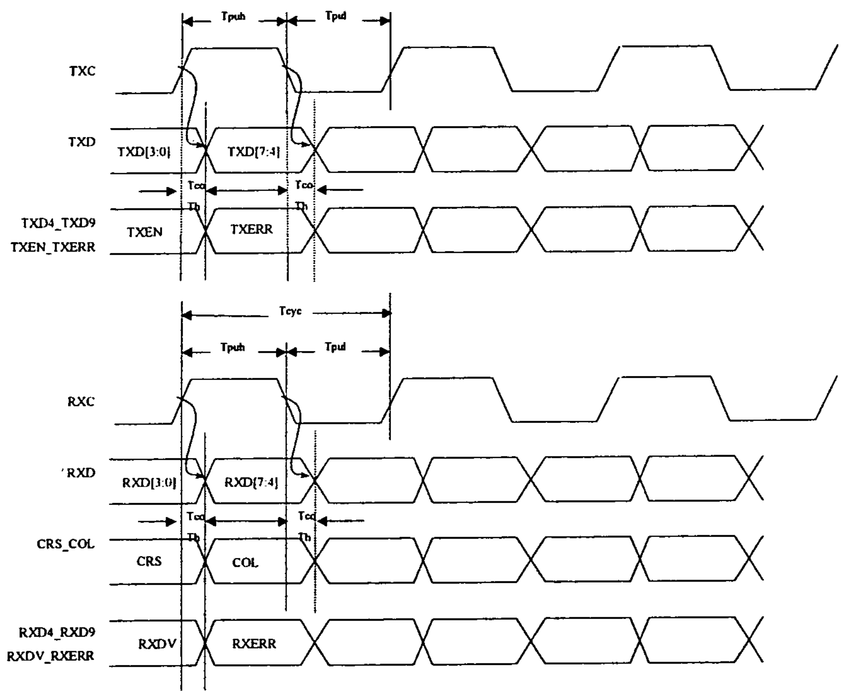

FIGURE 2

3.3 Timing Specifics (Measured with a 20pF / 1KΩ shunt load with a timing threshold of 1.25v)

Symbol	Parameter	Min	Typical	Max	Units
Tsu	Setup Time (at Receiver)	1.5			ns
Tco	Clock to Output Delay (at Transmitter)	.5		1.5	ns
Thold	Hold Time (at Receiver)	0			ns
Tcyc	Clock Cycle Duration	7.5	8	8.5	ns
Tpuh	Positive Pulse Width	3.8	4	4.2	ns
Tpul	Negative Pulse Width	3.8	4	4.2	ns
Tr / Tf	Rise / Fall Time (20-80%)			.75	ns

TABLE 3

3.4 SMII Functionality

This interface can be used to implement the 10/100 Mbps Ethernet Serial Media Independent Interface (SMII) by using TXC, TXD, RXD signals at the 125MHz rate as specified in the SMII ver1.2 document and the SYNCH bit can be multiplexed upon the TXEN signal. Support for SMII version 2.1 can be implemented by using RXCLK for self-synchronous clocking.

3.5 Mode Selection

The decision about which mode of operation this interface will use is left to the implementers. It may be done with hard-wired pins, or through register bits that are controlled by software.

3.6 Intellectual Property

The Hewlett-Packard Company has released its proprietary rights to information contained in this document to encourage others to adopt this interface as an industry standard. Any questions concerning this release should be directed to the Director of Intellectual Property, Hewlett-Packard Company, 3000 Hanover Street, Palo Alto, CA.

invent

Reduced Gigabit Media Independent Interface (RGMII)

6/1/2000
Version 1.0

Reduced Pin-count Interface
For
Gigabit Ethernet Physical Layer Devices

Revision Level	Date	Revision Description
1.0	**June 1, 2000**	**Released for public review and comment**

Exhibit 6

1.0 Purpose

The RGMII is intended to be an alternative to both the IEEE802.3z GMII and the TBI. The principle objective is to reduce the number of pins required to interconnect the MAC and the PHY from a maximum of 28 pins (TBI) to 13 pins in a cost effective and technology independent manner. In order to accomplish this objective, the data paths and all associated control signals will be reduced and control signals will be multiplexed together and both edges of the 125MHz clock will be used.

2.0 System Diagram

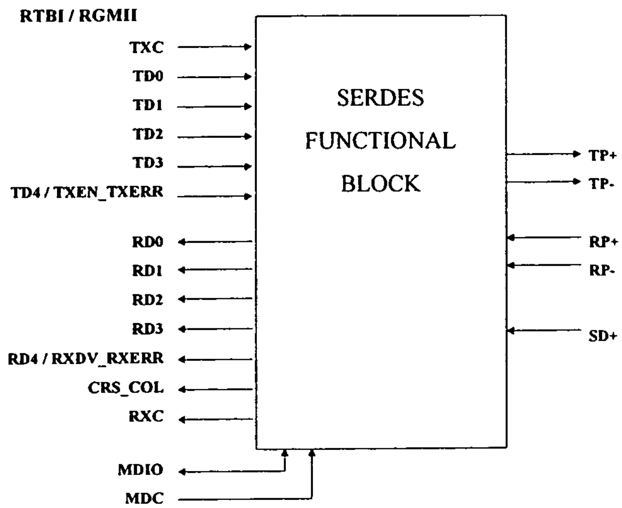

FIGURE 1 (System Diagram)

3.0 Signal Definitions

The RGMII will share four data path signals with the Reduced Ten Bit Interface (RTBI) and share control functionality with the fifth data signal. With the inclusion of the MDIO/MDC serial management signals, the RTBI will not require independent control signals like LK_REF, BYTE_EN, etc.

Signal Name	RTBI	RGMII	Description
TXC	**MAC**	**MAC**	The transmit reference clock will be 125Mhz, +-50ppm with a maximum pk-pk jitter of 100ps.
TD[3:0]	**PCS**	**MAC**	In RTBI mode, contains bits 3:0 on ↑ of TXC and bits 8:5 on ↓ of TXC. In RGMII mode, bits 3:0 on ↑ of TXC, bits7:4 on ↓ of TXC
TD[4]_TD[9] TXEN_TXERR	**PCS**	**MAC**	In RTBI mode, contains the fifth bit on ↑ of TXC and tenth bit on ↓ of TXC. In RGMII mode, TXEN on ↑ of TXC, TXERR on ↓ of TXC
RXC	**PHY**	**PHY**	The receive reference clock will be 125Mhz, +-50ppm. (May be derived from TXC)
RD[3:0]	**PHY**	**PHY**	In RTBI mode, contains bits 3:0 on ↑ of RXC and bits 8:5 on ↓ of RXC. In RGMII mode, bits 3:0 on ↑ of RXC, bits7:4 on ↓ of RXC
RD[4] _RD[9] RXDV_RXERR	**PHY**	**PHY**	In RTBI mode, contains the fifth bit on ↑ of RXC and tenth bit on ↓ of RXC. In RGMII mode, RXDV on ↑ of TXC, RXERR on ↓ of TXC
CRS_COL	N/A	**PHY (OPT*)**	CRS on ↑ of TXC, COL on ↓ of TXC

* CRS_COL required for half-duplex implementations only

TABLE 1

3.1 Electrical Characteristics

The RGMII and RTBI signals will be based upon 2.5v CMOS interface voltages.

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -1.0mA; V_{CC} = Min	2.1	VDD+.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.0mA; V_{CC}=Min	GND-.3	0.40	V
V_{IH}	Input High Voltage	V_{IH} > V_{IH} *Min*; V_{CC}=Min	1.7	–	V
V_{IL}	Input Low Voltage	V_{IH} > V_{IL} *Max*; V_{CC}=Min	-	.70	V
I_{IH}	Input High Current	V_{CC} = Max; V_{IN} = 2.5V	-	15	iA
I_{IL}	Input Low Current	V_{CC} = Max; V_{IN} = 0.4V	-15	-	iA

TABLE 2

3.2 Multiplexing of Data and Control

Multiplexing of data and control information is done by taking advantage of both edges of the reference clocks, then sending the lower 4 bits on the ↑ edge and the upper 4 bits on the ↓ edge. Control signals can be multiplexed into a single 125MHz clock cycle using the same technique.

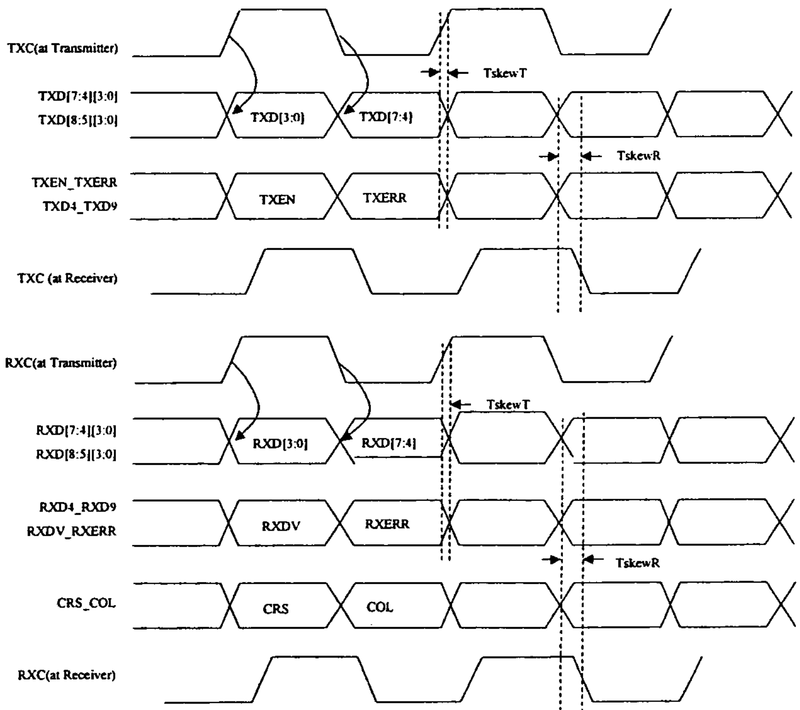

FIGURE 2

3.3 Timing Specifics (Measured with a 10pF / 1KΩ shunt load with a timing threshold of 1.25v)

Timing for this interface will be such that the clock and data are generated simultaneously by the source of the signals and therefore skew between the clock and data is critical to proper operation. This approach is being used to provide tighter control of skew.

Symbol	Parameter	Min	Typical	Max	Units
TskewT	Clock to Data output Skew (at Transmitter)	-500	0	500	ps
TskewR	Clock to Data input Skew (at Receiver) *note 1	1.0		2.0	ns
Tcyc	Clock Cycle Duration	7.5	8	8.5	ns
Tpuh	Positive Pulse Width	3.8	4	4.2	ns
Tpul	Negative Pulse Width	3.8	4	4.2	ns
Tr / Tf	Rise / Fall Time (20-80%)			.75	ns

note 1: This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns will be added to the associated clock signal.

TABLE 3

3.4 SMII Functionality

This interface can be used to implement the 10/100 Mbps Ethernet Serial Media Independent Interface (SMII) by using TXC, TXD, RXD signals at the 125MHz rate as specified in the SMII ver1.2 document and the SYNCH bit can be multiplexed upon the TXEN signal. Support for SMII version 2.1 may be implemented by using RXCLK for self-synchronous clocking, but it is optional.

3.5 Mode Selection

The decision about which mode of operation this interface will use is left to the implementers. It may be done with hard-wired pins, or through register bits that are controlled by software.

3.6 Intellectual Property

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Reduced Gigabit Media Independent Interface (RGMII)

8/1/2000
Version 1.1

Reduced Pin-count Interface
For
Gigabit Ethernet Physical Layer Devices

Revision Level	Date	Revision Description
1.0	June 1, 2000	Released for public review and comment
1.1	August 1, 2000	a) Modified RXERR and TXERR coding to reduce transitions and power in normal conditions. b) Modified timing diagram to incorporate PC board load conditions. c) Modified SMII description to add details for synchronous SMII. d) Modified Intellectual Property statement to address incorporation of IP from multiple sources. e) Modified document formatting.

Exhibit 7

1.0 Purpose

The RGMII is intended to be an alternative to both the IEEE802.3z GMII and the TBI. The principle objective is to reduce the number of pins required to interconnect the MAC and the PHY from a maximum of 28 pins (TBI) to 13 pins in a cost effective and technology independent manner. In order to accomplish this objective, the data paths and all associated control signals will be reduced and control signals will be multiplexed together and both edges of the 125MHz clock will be used.

2.0 System Diagram

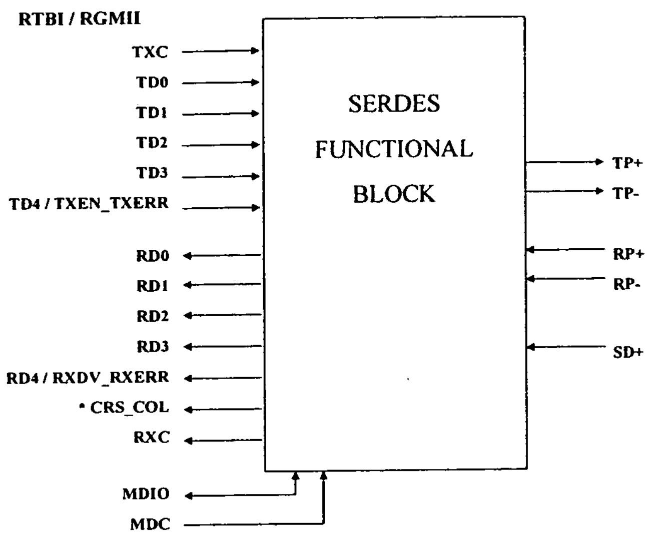

FIGURE 1 (System Diagram)

3.0 Signal Definitions

The RGMII will share four data path signals with the Reduced Ten Bit Interface (RTBI) and share control functionality with the fifth data signal. With the inclusion of the MDIO/MDC serial management signals, the RTBI will not require independent control signals like LK_REF, BYTE_EN, etc.

Signal Name	RTBI	RGMII	Description
TXC	**MAC**	**MAC**	The transmit reference clock will be 125Mhz, +- 50ppm with a maximum pk-pk jitter of 100ps.
TD[3:0]	**PCS**	**MAC**	In RTBI mode, contains bits 3:0 on ↑ of TXC and bits 8:5 on ↓ of TXC. In RGMII mode, bits 3:0 on ↑ of TXC, bits7:4 on ↓ of TXC
TD[4]_TD[9] TXEN_TXERR	**PCS**	**MAC**	In RTBI mode, contains the fifth bit on ↑ of TXC and tenth bit on ↓ of TXC. In RGMII mode, TXEN on ↑ of TXC, TXERR on ↓ of TXC
RXC	**PHY**	**PHY**	The receive reference clock will be 125Mhz, +- 50ppm. (May be derived from TXC)
RD[3:0]	**PHY**	**PHY**	In RTBI mode, contains bits 3:0 on ↑ of RXC and bits 8:5 on ↓ of RXC. In RGMII mode, bits 3:0 on ↑ of RXC, bits7:4 on ↓ of RXC
RD[4]_RD[9] RXDV_RXERR	**PHY**	**PHY**	In RTBI mode, contains the fifth bit on ↑ of RXC and tenth bit on ↓ of RXC. In RGMII mode, RXDV on ↑ of TXC, RXERR on ↓ of TXC
CRS_COL	N/A	**PHY (OPT*)**	CRS on ↑ of TXC, COL on ↓ of TXC

* CRS_COL required for half-duplex implementations only

TABLE 1 (Signal Definitions)

3.1 Signal Logic Conventions

All signals shall be conveyed with positive logic except as specified differently. For example, RXDV shall assume a valid voltage level greater than V_{OH_MIN} when true, and a valid voltage level less than V_{OL_MAX} when false.

3.2 Multiplexing of Data and Control

Multiplexing of data and control information is done by taking advantage of both edges of the reference clocks, then sending the lower 4 bits on the ↑ edge and the upper 4 bits on the ↓ edge. Control signals can be multiplexed into a single 125MHz clock cycle using the same technique.

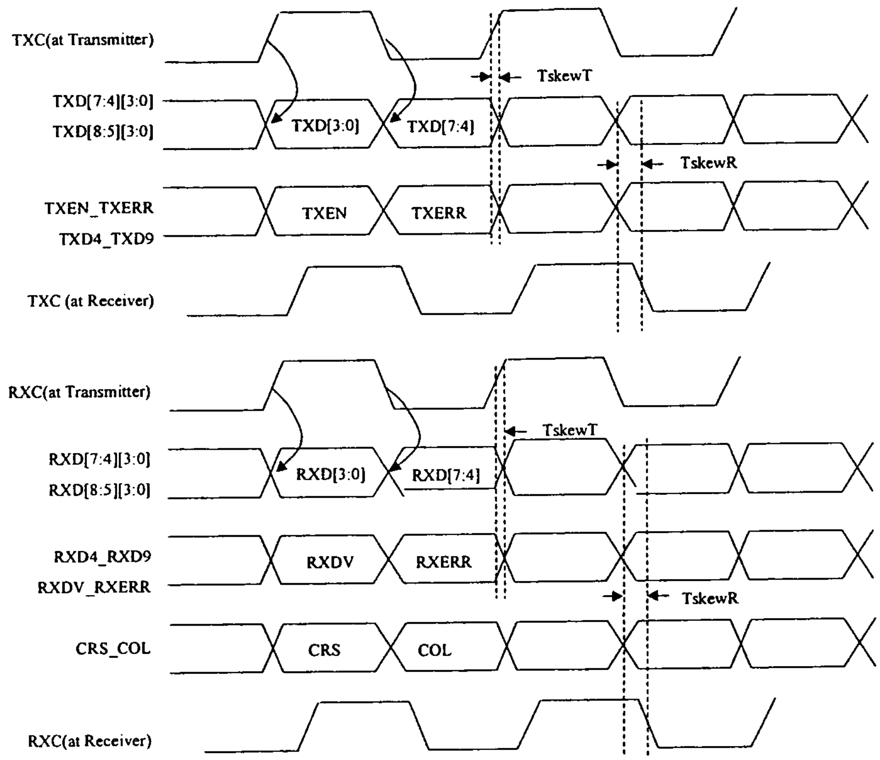

FIGURE 2 (Multiplexing & Timing Diagram)

3.3 Timing Specifics (Measured with the circuit shown in FIGURE 3 and a timing threshold voltage of 1.25v)

Timing for this interface will be such that the clock and data are generated simultaneously by the source of the signals and therefore skew between the clock and data is critical to proper operation. This approach is being used to provide tighter control of skew.

Symbol	Parameter	Min	Typical	Max	Units
TskewT	Clock to Data output Skew (at Transmitter)	-500	0	500	ps
TskewR	Clock to Data input Skew (at Receiver) *note 1	1.0		2.0	ns
Tcyc	Clock Cycle Duration	7.5	8	8.5	ns
Tpuh	Positive Pulse Width	3.8	4	4.2	ns
Tpul	Negative Pulse Width	3.8	4	4.2	ns
Tr / Tf	Rise / Fall Time (20-80%)			.75	ns

note 1: This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns will be added to the associated clock signal.

TABLE 2

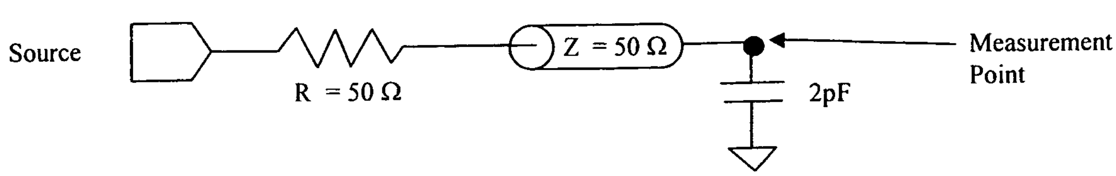

FIGURE 3

3.4 TXERR and RXERR Coding

To reduce power of this interface, TXERR and RXERR will be encoded in a manner that minimizes transitions during normal network operation. This is done by the following encoding method.

TXERR <= TXERR (XOR) TXEN
RXERR <= RXERR (XOR) RXDV

When receiving a valid frame with no errors, RXDV=true is generated as a valid (greater than V_{OH_MIN}) voltage on the ↑ edge of RXCLK and RXERR=false is generated as a valid (greater than V_{OH_MIN}) voltage on the ↓ edge of RXCLK. When no frame is being received, RXDV=false is generated as a valid (less than V_{OL_MAX}) voltage on the ↑ edge of RXCLK and RXERR=false is generated as a valid (less than V_{OL_MAX}) voltage on the ↓ edge of RXCLK.

When receiving a valid frame with errors, RXDV=true is generated as valid (greater than V_{OH_MIN}) voltage on the ↑ edge of RXCLK and RXERR=true is generated as a valid (less than V_{OL_MAX}) voltage on the ↓ edge of RXCLK.

TXERR is treated in a similar manner. During normal frame transmission, the signal stays high for both edges of the clock and during the period between frames where no errors are to be indicated, the signal stays low for both edges.

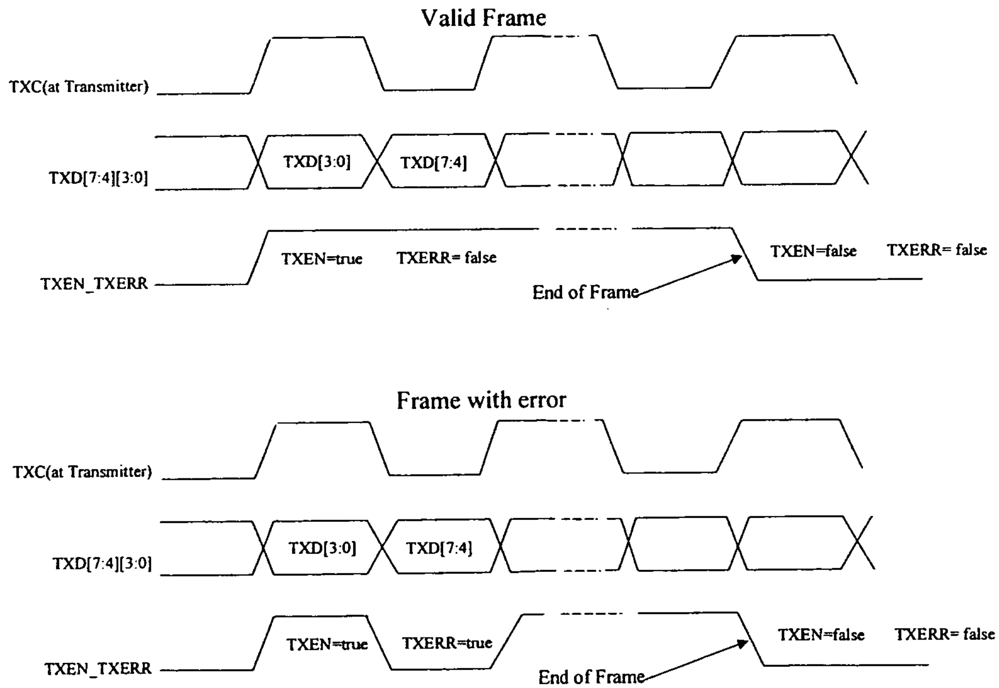

FIGURE 4

3.5 Electrical Characteristics

The RGMII and RTBI signals will be based upon 2.5v CMOS interface voltages.

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -1.0mA; V_{CC} = Min	2.1	VDD+.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.0mA; V_{CC}=Min	GND-.3	0.40	V
V_{IH}	Input High Voltage	V_{IH} > V_{IH} *Min*; V_{CC}=Min	1.7	–	V
V_{IL}	Input Low Voltage	V_{IH} > V_{IL} *Max*; V_{CC}=Min	-	.70	V
I_{IH}	Input High Current	V_{CC} = Max; V_{IN} = 2.5V	-	15	µA
I_{IL}	Input Low Current	V_{CC} = Max; V_{IN} = 0.4V	-15	-	µA

TABLE 3

4.0 SMII Functionality

This interface can be used to implement the 10/100 Mbps Ethernet Serial Media Independent Interface (SMII) by using TXC, TXD, RXD signals at the 125MHz rate as specified in the SMII ver1.2 document and the SYNCH bit can be multiplexed upon the TXEN signal. Support for SMII version 2.1 may be implemented by using RXCLK for self-synchronous clocking, but it is optional. When implemented, the following pin mapping will apply.

RGMII Signal	SMII v1.2 Signal	SMII v2.1 signal
TXEN_TXERR	SYNC	T_SYNC
TD[0]	TD	TD
RXDV_RXERR	n/a	R_SYNC
RD[0]	RD	RD
TXC	TCK	TCK
RXC	n/a	RCK

TABLE 4

5.0 Mode Selection

The decision about which mode of operation this interface will use is left to the implementers. It may be done with hard-wired pins, or through register bits that are controlled by software.

6.0 Hewlett Packard Intellectual Property

The Hewlett-Packard Company has released its proprietary rights to information contained in this document to encourage others to adopt this interface as an industry standard. Any company wishing to use this specification may do so if they will in turn relinquish their proprietary rights to information contained or referenced herein. Any questions concerning this release should be directed to the Director of Intellectual Property, Hewlett-Packard Company, 3000 Hanover Street, Palo Alto, CA.

6.1 Contributions of Intellectual Property

All contributing companies incorporating their logo on this document have relinquished their proprietary rights to information contained in this document to encourage others to adopt this interface as an industry standard. Any questions concerning their contributions should be directed to their corporate headquarters.

Marvell Semiconductor Confidential

Marvell Semiconductor proposed changes to HP-RGMII
7/25/00
William Lo

All RGMII changes should be a simple exercise in combinatorial mapping.

Goals:
1) Keep the 10/100/1000 mapping consistent
2) 12 pin interface
3) Easy migration to RGMII in 10/100 mode from existing MII
4) Minimize pin toggling to save power

Change #1
Let RXDV_RXERR and TXEN_TXERR be single data rate signal.
in all 3 speeds.
Probably a good idea to rename it to RX_CTRL and TX_CTRL.

RD[3:0] and TD[3:0] double datarate in 1000Mb/s,
single data rate in 10/100.

Change #2
IEEE TX_CLK eliminated in 10/100.
GTX_CLK operates at 125Mhz, 25Mhz, 2.5Mhz in 1000/100/10 respectively.

RX_CLK operates same way as in GMII/MII

Change #3
Do combinatorial mapping as follows

GMII/MII			RGMII (HP-Marvell)		
TXEN	TXER	TXD[7:0]	TX_CTRL	TD[3:0]	
0	0	xxxxxxxx	0	0xxx	Idle
0	1	00001111	0	1001	Carrier Extension
0	1	00011111	0	1011	Carrier Extension Error
1	0	xxxxxxxx	1	xxxx	Data
1	1	xxxxxxxx	0	1100	Symbol Error

GMII/MII				RGMII (HP-Marvell)		
CRS	RXDV	RXER	RXD[7:0]	RX_CTRL	RD[3:0]	
0	0	0	xxxxxxxx	0	0xxx	Idle
1	0	0	xxxxxxxx	0	1111	Carrier sense no data
1	0	1	00001110	0	1000	False Carrier
1	0	1	00001111	0	1001	Carrier Extension
1	0	1	00011111	0	1011	Carrier Extension Error
1	1	0	xxxxxxxx	1	xxxx	Data
1	1	1	xxxxxxxx	0	1100	Symbol Error

This change may be a pain for someone who already implemented
the RGMII v 1.0 for 1000Mb/s already but if this mapping is adopted then
the advantages are
A) eliminates double data rate signals in the 10/100 case - hence no timing
   change in MII.
B) no excessive toggling of the control pin in Carrier extension,
   Carrier extension error, false carrier, or symbol error cases
C) Consistent mapping across 10/100/1000

Change #4
Eliminate CRS_COL pin

Exhibit 8

Timing
In 1000Mb/s mode keep things the way it is now.

In 10/100.

On the RX side keep the same as IEEE with 10ns setup and hold relative to rising edge of RX_CLK. Trace delay should not really be an issue.

On the TX side since GTX_CLK is the source make it like the GMII with 2.0ns setup and 0ns hold at the receiving side. However since there is trace delays to take into account and there is no reason to make this so tight when the fastest clock is 40ns I would suggest loosening the spec.

Make it real loose for both PHY and MAC. Trace delay a no brainer if 1000Mb/s timings satisfied.

A) At the source relative to rising edge of TX_CLK or RX_CLK
   Setup time 10ns, hold 10ns.

B) At the sink relative to the rising edge of TX_CLK or RX_CLK
   Setup time 7ns, hold 7ns.

REVIEW ONLY 1.1

i n v e n t

Reduced Gigabit Media Independent Interface (RGMII)

8/1/2000

Version 1.1-b

Reduced Pin-count Interface For Gigabit Ethernet Physical Layer Devices

Revision Level	Date	Revision Description
1.0	June 1, 2000	Released for public review and comment
1.1	August 1, 2000	a) Modified RXERR and TXERR coding to reduce transitions and power in normal conditions. b) Removed CRS_COL pin and incorporated coding alternative for half duplex implementation. c) Found and corrected some inconsistencies in which clock was specified for timing. PHY generated signals are based on RXC and MAC generated signals are based on TXC. Specified that RXC is derived from TXC to eliminate need for FIFOs in the MAC. d) Modified timing diagram to incorporate PC board load conditions. e) Removed references to SMII due to broad concerns about IP exclusivity and added specification for 10/100 MII operation. f) Modified Intellectual Property statement to address incorporation of IP from multiple sources. g) Modified document formatting.

Exhibit 9

1.0 Purpose

The RGMII is intended to be an alternative to the IEEE802.3u MII, the IEEE802.3z GMII and the TBI. The principle objective is to reduce the number of pins required to interconnect the MAC and the PHY from a maximum of 28 pins (TBI) to 12 pins in a cost effective and technology independent manner. In order to accomplish this objective, the data paths and all associated control signals will be reduced and control signals will be multiplexed together and both edges of the 125MHz clock will be used.

2.0 System Diagram

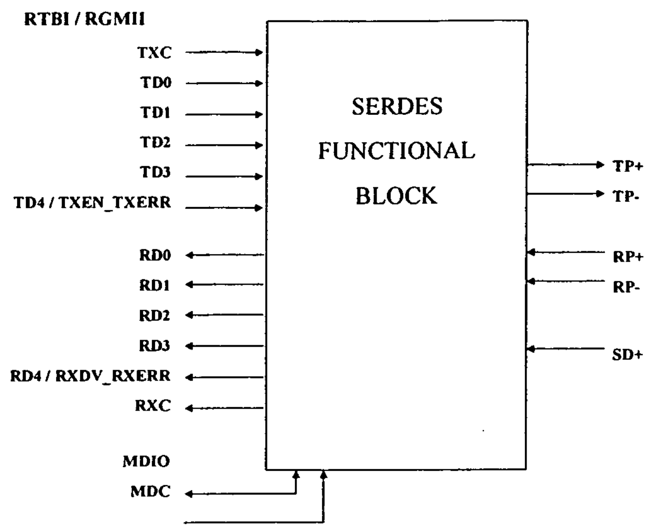

FIGURE 1 (System Diagram)

3.0 Signal Definitions

The RGMII will share four data path signals with the Reduced Ten Bit Interface (RTBI) and share control functionality with the fifth data signal. With the inclusion of the MDIO/MDC serial management signals, the RTBI will not require independent control signals like LK_REF, BYTE_EN, etc. Register assignment of SERDES control bits is left to the implementer.

Signal Name	RTBI	RGMII	Description
TXC	MAC	MAC	The transmit reference clock will be 125Mhz, +- 50ppm with a maximum pk-pk jitter of 100ps.
TD[3:0]	PCS	MAC	In RTBI mode, contains bits 3:0 on ↑ of TXC and bits 8:5 on ↓ of TXC. In RGMII mode, bits 3:0 on ↑ of TXC, bits7:4 on ↓ of TXC
TD[4]_TD[9] TXEN_TXERR	PCS	MAC	In RTBI mode, contains the fifth bit on ↑ of TXC and tenth bit on ↓ of TXC. In RGMII mode, TXEN on ↑ of TXC, TXERR on ↓ of TXC
RXC	PHY	PHY	The receive reference clock will be 125Mhz, +- 50ppm. and shall be derived from TXC.
RD[3:0]	PHY	PHY	In RTBI mode, contains bits 3:0 on ↑ of RXC and bits 8:5 on ↓ of RXC. In RGMII mode, bits 3:0 on ↑ of RXC, bits7:4 on ↓ of RXC
RD[4] _RD[9] RXDV_ RXERR	PHY	PHY	In RTBI mode, contains the fifth bit on ↑ of RXC and tenth bit on ↓ of RXC. In RGMII mode, RXDV on ↑ of RXC, RXERR on ↓ of RXC

TABLE 1 (Signal Definitions)

3.1 Signal Logic Conventions

All signals shall be conveyed with positive logic except as specified differently. For descriptive purposes, a signal shall be at a logic "high" when it is at a valid voltage level greater than V_{OH_MIN}, and logic "low" when it is at a valid voltage level less than V_{OL_MAX}.

3.2 Multiplexing of Data and Control

Multiplexing of data and control information is done by taking advantage of both edges of the reference clocks and sending the lower 4 bits on the ↑ edge and the upper 4 bits on the ↓ edge. Control signals can be multiplexed into a single 125MHz clock cycle using the same technique.

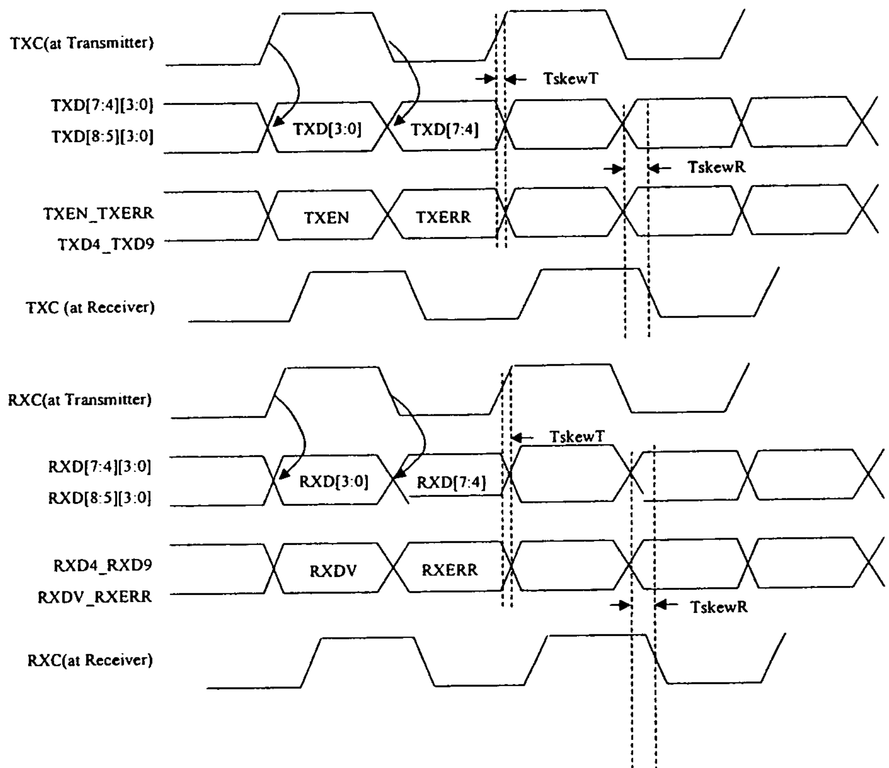

FIGURE 2 (Multiplexing & Timing Diagram)

3.3 Timing Specifics (Measured with the circuit shown in FIGURE 3 and a timing threshold voltage of 1.25v)

Timing for this interface will be such that the clock and data are generated simultaneously by the source of the signals and therefore skew between the clock and data is critical to proper operation. This approach is being used to provide tighter control of skew. Timing values are defined in percentages of the nominal clock period so to make this table speed independent.

Symbol	Parameter	Min	Typical	Max	Units
TskewT	Clock to Data output Skew (at Transmitter)	-5	0	5	%
TskewR	Clock to Data input Skew (at Receiver) *note 1,2	1		2	ns
Tcyc	Clock Cycle Duration	90	100	110	%
Tpuh	Positive Pulse Width	45	50	55	%
Tpul	Negative Pulse Width	45	50	55	%
Tr / Tf	Rise / Fall Time (20-80%)			10	%

note 1: This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns will be added to the associated clock signal.

note 2: For 10Mbps and 100Mbps and 1000 speeds, Tcyc will scale to 400ns and 40ns and 8ns respectively.

TABLE 2

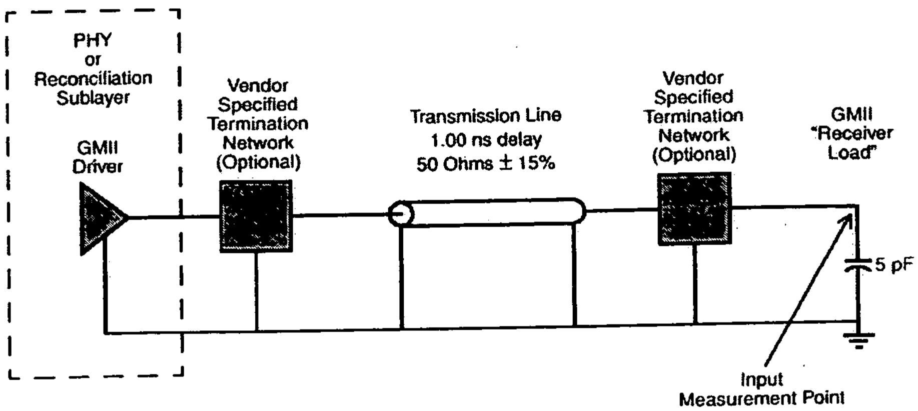

FIGURE 3

3.4 TXERR and RXERR and CRS Coding

To reduce power of this interface, TXERR and RXERR, will be encoded in a manner that minimizes transitions during normal network operation. This is done by the following encoding method. Note that the value of GMII_TX_ER and GMII_TX_EN are valid at the rising edge of the clock while TXERR is presented on the falling edge of the clock. RXERR coding behaves in the same way.

TXERR <= GMII_TX_ER (XOR) GMII_TX_EN
RXERR <= GMII_RX_ER (XOR) GMII_RX_DV

When receiving a valid frame with no errors, RXDV=true is generated as a logic high on the ↑ edge of RXC and RXERR=false is generated as a logic high the ↓ edge of RXC. When no frame is being received, RXDV=false is generated as a logic low on the ↑ edge of RXC and RXERR=false is generated as a logic low on the ↓ edge of RXC.

When receiving a valid frame with errors, RXDV=true is generated as logic high on the ↑ edge of RXC and RXERR=true is generated as a logic low on the ↓ edge of RXC.

TXERR is treated in a similar manner. During normal frame transmission, the signal stays at a logic high for both edges of TXC and during the period between frames where no errors are to be indicated, the signal stays low for both edges.

TXEN	TXERR	TXD[7:0]	Description	PLS_DATA.request parameter
0	0	00 through FF	Normal inter-frame	TRANSMIT_COMPLETE
0	1	00 through 0E	Reserved —	
0	1	0F	Carrier Extend	EXTEND (eight bits)
0	1	10 through 1E	Reserved —	
0	1	1F	Carrier Extend Error	EXTEND_ERROR (eight bits)
0	1	20 through FE	Reserved —	
1	0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1	1	00 through FF	Transmit error propagation	No applicable parameter

NOTE—Values in TXD[7:0] column are in hexadecimal

TABLE 3 (Allowable Encoding of TXD, TXERR and TXEN)

RXDV	RXERR	RXD[7:0]	Description	PLS_DATA.indicate parameter
0	0	00 through FF	Normal inter-frame	No applicable parameter
0	1	00	Normal inter-frame	No applicable parameter
0	1	01through 0D	Reserved	—
0	1	0E	False Carrier indication	No applicableparameter
0	1	0F	Carrier Extend	EXTEND (eight bits)
0	1	10 through 1E	Reserved	—
0	1	1F	Carrier Extend Error	ZERO, ONE (eight bits)
0	1	20 through FE	Reserved	—
0	1	FF	Carrier Sense	PLS_Carrier.Indicate
1	0	00 through FF	Normal data reception	ZERO, ONE (eight bits)
1	1	00 through FF	Data reception error	ZERO, ONE(eight bits)

NOTE—Values in RXD<7:0> column are in hexadecimal.

TABLE 4 (Allowable Encoding of RXD, RXDV and RXERR)

In half duplex mode, CRS is indicated by the case where RXDV is true, or the case where RXDV is false, RXERR is true, and a value of FF exists on the RXD[7:0] bits simultaneously or in the case where a Carrier Extend, Carrier Extend Error or False Carrier are occurring.

Collision is determined at the MAC by the assertion of TXEN being true while CRS or RXDV are true at the same time. The PHY will not assert CRS as a result of TXEN being true.

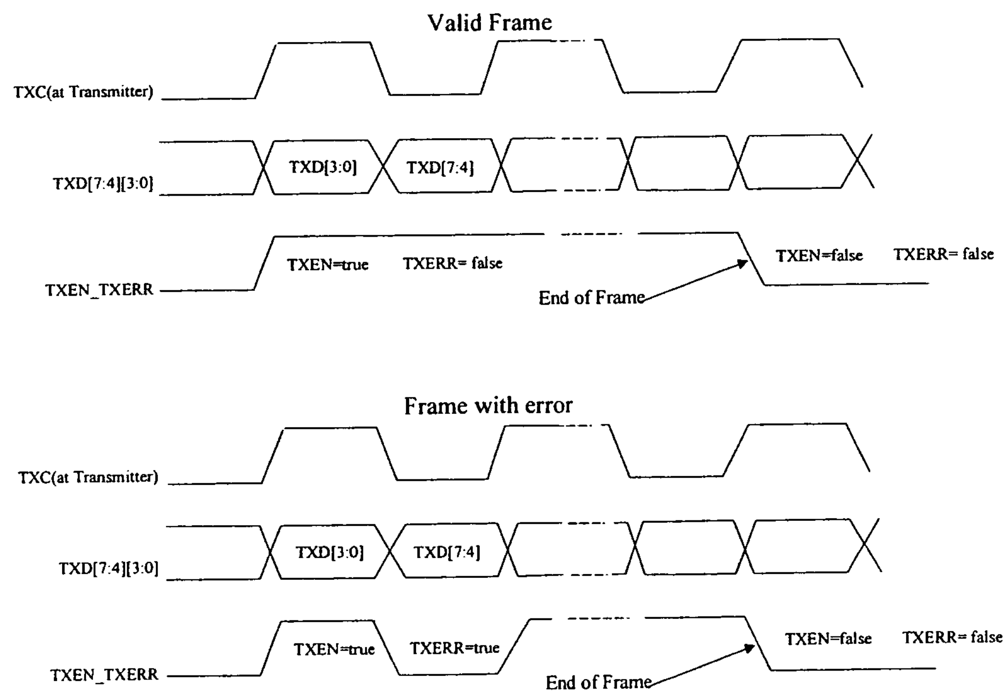

FIGURE 4

3.5 Electrical Characteristics

The RGMII and RTBI signals will be based upon 2.5v CMOS interface voltages.

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -1.0mA; V_{CC} = Min	2.1	VDD+.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.0mA; V_{CC}=Min	GND-.3	0.40	V
V_{IH}	Input High Voltage	V_{IH} > V_{IH}_Min; V_{CC}=Min	1.7	–	V
V_{IL}	Input Low Voltage	V_{IH} > V_{IL}_Max; V_{CC}=Min	-	.70	V
I_{IH}	Input High Current	V_{CC} = Max; V_{IN} = 2.5V	-	15	uA
I_{IL}	Input Low Current	V_{CC} = Max; V_{IN} = 0.4V	-15	-	uA

TABLE 5

4.0 10/100 Functionality

This interface can be used to implement the 10/100 Mbps Ethernet Media Independent Interface (MII) by reducing the clock rate to 25MHz for 100Mbps operation and 2.5MHz for 10Mbps. The TXC will always be generated by the MAC and RXC will be generated by the PHY.

This interface will operate at 10 and 100Mbps speeds exactly the same way it does at Gigabit speed with the exception that the data is duplicated on the ↓ edge of the appropriate clock.

For 10 and 100 speeds, CRS will be asserted asynchronously upon detection of carrier unlike Gigabit speed where CRS will be asserted synchronous to the RXC.

5.0 Mode Selection

The decision about which mode of operation this interface will use is left to the implementers. It may be done with hard-wired pins, or through register bits that are controlled by software.

6.0 Hewlett Packard Intellectual Property

The Hewlett-Packard Company has released its proprietary rights to information contained in this document to encourage others to adopt this interface as an industry standard. Any company wishing to use this specification may do so if they will in turn relinquish their proprietary rights to information contained or referenced herein. Any questions concerning this release should be directed to the Director of Intellectual Property, Hewlett-Packard Company, 3000 Hanover Street, Palo Alto, CA.

6.1 Contributions of Intellectual Property

All contributing companies incorporating their logo on this document have relinquished their proprietary rights to information contained in this document to encourage others to adopt this interface as an industry standard. Any questions concerning their contributions should be directed to their corporate headquarters.

REVIEW ONLY 1.2

invent

Reduced Gigabit Media Independent Interface (RGMII)

8/10/2000
Version 1.2

Reduced Pin-count Interface
For
Gigabit Ethernet Physical Layer Devices

Exhibit 10

Preliminary Draft for review only

Revision Level	Date	Revision Description
1.0	June 1, 2000	Released for public review and comment
1.1	August 1, 2000	a) Modified RXERR and TXERR coding to reduce transitions and power in normal conditions. b) Removed CRS_COL pin and incorporated coding alternative for half duplex implementation. c) Found and corrected some inconsistencies in which clock was specified for timing. PHY generated signals are based on RXC and MAC generated signals are based on TXC. Specified that RXC is derived from TXC to eliminate need for FIFOs in the MAC. d) Modified timing diagram to incorporate PC board load conditions. e) Removed references to SMII due to broad concerns about IP exclusivity and added specification for 10/100 MII operation. f) Modified Intellectual Property statement to address incorporation of IP from multiple sources. g) Modified document formatting.
1.2	August 10, 2000	a) Required CRS assertion/deassertion to be synchronous for all speeds. b) Returned timing numbers to absolute from percentages. c) Added verbage to allow clock cycle stretching during speed changes and receive data and clock acquistion. d) Slight wording change on IP statements to limit scope.

1.0 Purpose

The RGMII is intended to be an alternative to the IEEE802.3u MII, the IEEE802.3z GMII and the TBI. The principle objective is to reduce the number of pins required to interconnect the MAC and the PHY from a maximum of 28 pins (TBI) to 12 pins in a cost effective and technology independent manner. In order to accomplish this objective, the data paths and all associated control signals will be reduced and control signals will be multiplexed together and both edges of the clock will be used. For Gigabit operation, the clocks will operate at 125MHz, and for 10/100 operation, the clocks will operate at 2.5MHz or 25MHz respectively.

2.0 System Diagram

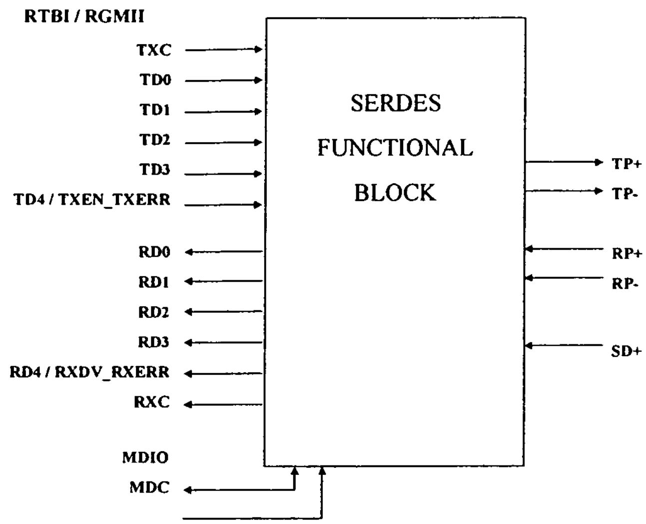

FIGURE 1 (System Diagram)

3.0 Signal Definitions

The RGMII will share four data path signals with the Reduced Ten Bit Interface (RTBI) and share control functionality with the fifth data signal. With the inclusion of the MDIO/MDC serial management signals, the RTBI will not require independent control signals like LK_REF, BYTE_EN, etc. Register assignment of SERDES control bits is left to the implementer.

Signal Name	RTBI	RGMII	Description
TXC	MAC	MAC	The transmit reference clock will be 125Mhz, +-50ppm with a maximum pk-pk jitter of 100ps.
TD[3:0]	PCS	MAC	In RTBI mode, contains bits 3:0 on ↑ of TXC and bits 8:5 on ↓ of TXC. In RGMII mode, bits 3:0 on ↑ of TXC, bits7:4 on ↓ of TXC
TD[4]_TD[9] TXEN_TXERR	PCS	MAC	In RTBI mode, contains the fifth bit on ↑ of TXC and tenth bit on ↓ of TXC. In RGMII mode, TXEN on ↑ of TXC, TXERR on ↓ of TXC
RXC	PHY	PHY	The receive reference clock will be 125Mhz, +-50ppm. and shall be derived from TXC.
RD[3:0]	PHY	PHY	In RTBI mode, contains bits 3:0 on ↑ of RXC and bits 8:5 on ↓ of RXC. In RGMII mode, bits 3:0 on ↑ of RXC, bits7:4 on ↓ of RXC
RD[4] _RD[9] RXDV_ RXERR	PHY	PHY	In RTBI mode, contains the fifth bit on ↑ of RXC and tenth bit on ↓ of RXC. In RGMII mode, RXDV on ↑ of RXC, RXERR on ↓ of RXC

TABLE 1 (Signal Definitions)

3.1 Signal Logic Conventions

All signals shall be conveyed with positive logic except as specified differently. For descriptive purposes, a signal shall be at a logic "high" when it is at a valid voltage level greater than V_{OH_MIN}, and logic "low" when it is at a valid voltage level less than V_{OL_MAX}.

3.2 Multiplexing of Data and Control

Multiplexing of data and control information is done by taking advantage of both edges of the reference clocks and sending the lower 4 bits on the ↑ edge and the upper 4 bits on the ↓ edge. Control signals can be multiplexed into a single clock cycle using the same technique.

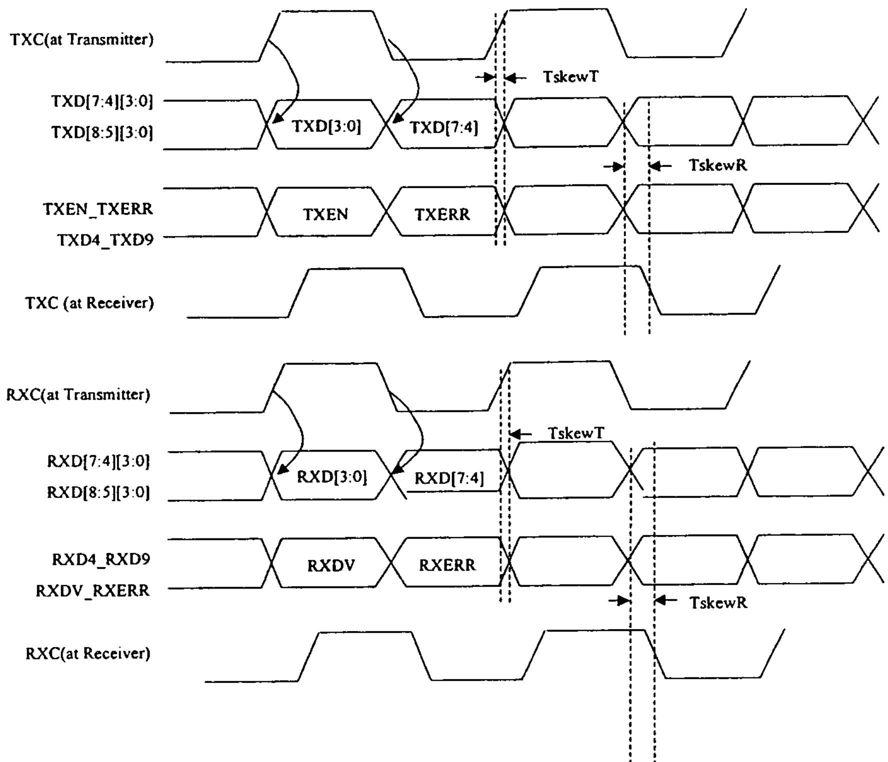

FIGURE 2 (Multiplexing & Timing Diagram)

3.3 Timing Specifics (Measured with the circuit shown in FIGURE 3 and a timing threshold voltage of 1.25v)

Timing for this interface will be such that the clock and data are generated simultaneously by the source of the signals and therefore skew between the clock and data is critical to proper operation. This approach is being used to provide tighter control of skew. Timing values are defined in percentages of the nominal clock period so to make this table speed independent.

Symbol	Parameter	Min	Typical	Max	Units
TskewT	Clock to Data output Skew (at Transmitter)	-500	0	500	ps
TskewR	Clock to Data input Skew (at Receiver) *note 1	1		2.8	ns
Tcyc	Clock Cycle Duration *note 2	7.2	8	8.8	ns
Tpuh	Positive Pulse Width *note 3	3.8	4.0	---	ns
Tpul	Negative Pulse Width *note 3	3.8	4.0	---	ns
Tr / Tf	Rise / Fall Time (20-80%)			.75	ns

note 1: This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns will be added to the associated clock signal.

note 2: For 10Mbps and 100Mbps, Tcyc will scale to 400ns and 40ns respectively.

note 3: For 10Mbps, Tpuh and Tpul may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum times are not violated.

TABLE 2

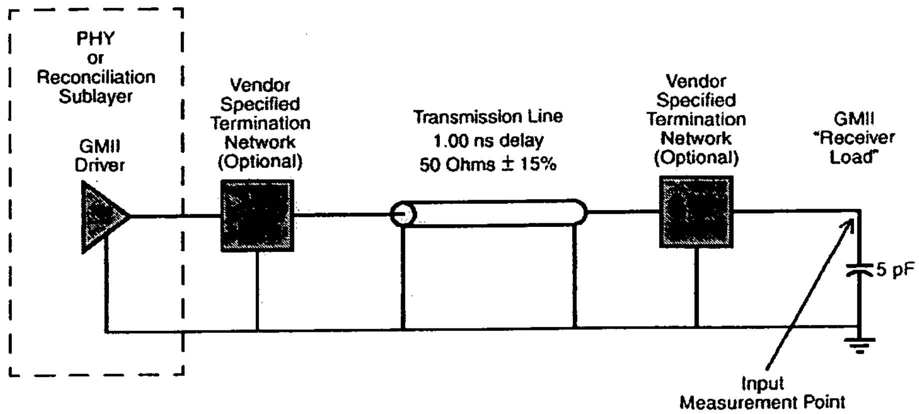

FIGURE 3

3.4 TXERR and RXERR Coding

To reduce power of this interface, TXERR and RXERR, will be encoded in a manner that minimizes transitions during normal network operation. This is done by the following encoding method. Note that the value of GMII_TX_ER and GMII_TX_EN are valid at the rising edge of the clock while TXERR is presented on the falling edge of the clock. RXERR coding behaves in the same way.

TXERR <= GMII_TX_ER (XOR) GMII_TX_EN
RXERR <= GMII_RX_ER (XOR) GMII_RX_DV

When receiving a valid frame with no errors, RXDV=true is generated as a logic high on the ↑ edge of RXC and RXERR=false is generated as a logic high the ↓ edge of RXC. When no frame is being received, RXDV=false is generated as a logic low on the ↑ edge of RXC and RXERR=false is generated as a logic low on the ↓ edge of RXC.

When receiving a valid frame with errors, RXDV=true is generated as logic high on the ↑ edge of RXC and RXERR=true is generated as a logic low on the ↓ edge of RXC.

TXERR is treated in a similar manner. During normal frame transmission, the signal stays at a logic high for both edges of TXC and during the period between frames where no errors are to be indicated, the signal stays low for both edges.

GMII_TX_EN	GMII_TX_ER	TXD[7:0]	Description	PLS_DATA.request parameter
0	0	00 through FF	Normal inter-frame	TRANSMIT_COMPLETE
0	1	00 through 0E	Reserved —	
0	1	0F	Carrier Extend	EXTEND (eight bits)
0	1	10 through 1E	Reserved —	
0	1	1F	Carrier Extend Error	EXTEND_ERROR (eight bits)
0	1	20 through FE	Reserved —	
1	0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1	1	00 through FF	Transmit error propagation	No applicable parameter

NOTE—Values in TXD[7:0] column are in hexadecimal

TABLE 3 (Allowable Encoding of TXD, TXERR and TXEN)

GMII_RX_DV	GMII_RX_ER	RXD[7:0]	Description	PLS_DATA.indicate parameter
0	0	00 through FF	Normal inter-frame	No applicable parameter
0	1	00	Normal inter-frame	No applicable parameter
0	1	01through 0D	Reserved	—
0	1	0E	False Carrier indication	No applicableparameter
0	1	0F	Carrier Extend	EXTEND (eight bits)
0	1	10 through 1E	Reserved	—
0	1	1F	Carrier Extend Error	ZERO, ONE (eight bits)
0	1	20 through FE	Reserved	—
0	1	FF	Carrier Sense	PLS_Carrier.Indicate
1	0	00 through FF	Normal data reception	ZERO, ONE (eight bits)
1	1	00 through FF	Data reception error	ZERO, ONE(eight bits)

NOTE—Values in RXD[7:0] column are in hexadecimal.

TABLE 4 (Allowable Encoding of RXD, RXDV and RXERR)

In half duplex mode, CRS is indicated by the case where RXDV is true, or the case where RXDV is false, RXERR is true, and a value of FF exists on the RXD[7:0] bits simultaneously or in the case where a Carrier Extend, Carrier Extend Error or False Carrier are occurring.

Collision is determined at the MAC by the assertion of TXEN being true while CRS or RXDV are true at the same time. The PHY will not assert CRS as a result of TXEN being true.

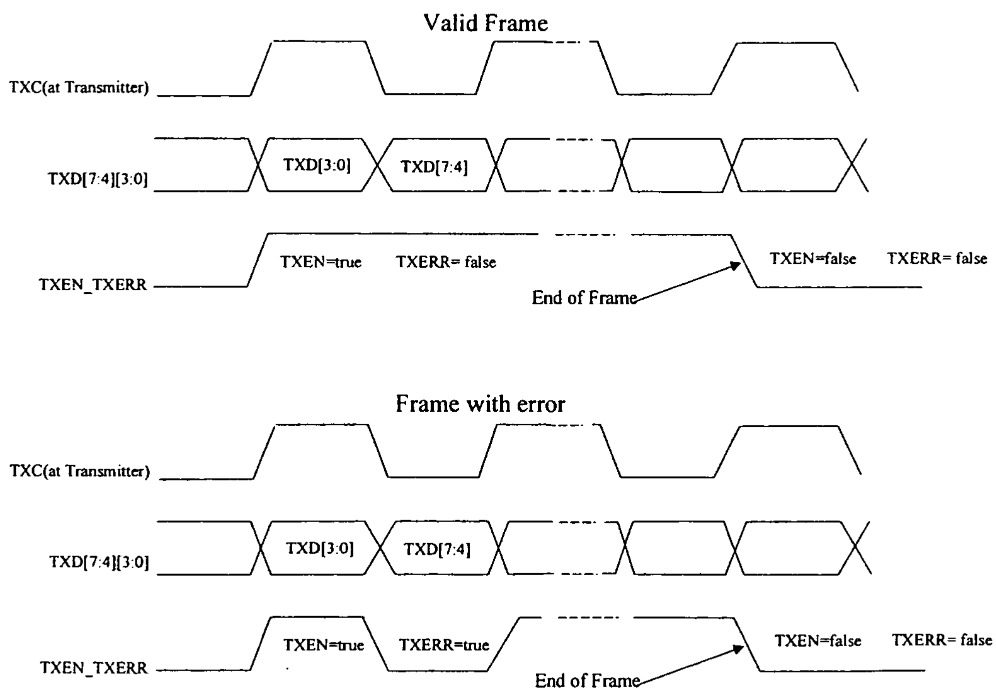

FIGURE 4

3.5 Electrical Characteristics

The RGMII and RTBI signals will be based upon 2.5v CMOS interface voltages.

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -1.0mA; V_{CC} = Min	2.1	VDD+.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.0mA; V_{CC}=Min	GND-.3	0.40	V
V_{IH}	Input High Voltage	V_{IH} > V_{IH}_Min; V_{CC}=Min	1.7	–	V
V_{IL}	Input Low Voltage	V_{IH} > V_{IL}_Max; V_{CC}=Min	-	.70	V
I_{IH}	Input High Current	V_{CC} = Max; V_{IN} = 2.5V	-	15	uA
I_{IL}	Input Low Current	V_{CC} = Max; V_{IN} = 0.4V	-15	-	uA

TABLE 5

4.0 10/100 Functionality

This interface can be used to implement the 10/100 Mbps Ethernet Media Independent Interface (MII) by reducing the clock rate to 25MHz for 100Mbps operation and 2.5MHz for 10Mbps. The TXC will always be generated by the MAC and RXC will be generated by the PHY. During packet reception, the RXC may be stretched on either the positive or negative pulse to accommodate the transition from the free running clock to a data-synchronous clock domain. When the speed of the PHY changes, a similar stretching of the positive or negative pulses is allowed. Minimum pulse widths must be maintained.

This interface will operate at 10 and 100Mbps speeds exactly the same way it does at Gigabit speed with the exception that the data is duplicated on the ↓ edge of the appropriate clock.

Mode Selection

The decision about which mode of operation this interface will use is left to the implementers. It may be done with hard-wired pins, or through register bits that are controlled by software.

The MAC will not assert TXEN or TXERR until it has ensured that it is operating at the same speed as the PHY.

5.0 Hewlett Packard Intellectual Property

The Hewlett-Packard Company has released its proprietary rights to information contained in this document for the express purpose of implementation of this specification, to encourage others to adopt this interface as an industry standard. Any company wishing to use this specification may do so if they will in turn relinquish their proprietary rights to information contained or referenced herein. Any questions concerning this release should be directed to the Director of Intellectual Property, Hewlett-Packard Company, 3000 Hanover Street, Palo Alto, CA.

5.1 Contributions of Intellectual Property

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Reduced Gigabit Media Independent Interface (RGMII)

9/11/2000
Version 1.2

Reduced Pin-count Interface
For
Gigabit Ethernet Physical Layer Devices

Preliminary Draft for review only

Exhibit 11

Revision Level	Date	Revision Description
1.0	June 1, 2000	Released for public review and comment
1.1	August 1, 2000	a) Modified RXERR and TXERR coding to reduce transitions and power in normal conditions. b) Removed CRS_COL pin and incorporated coding alternative for half duplex implementation. c) Found and corrected some inconsistencies in which clock was specified for timing. PHY generated signals are based on RXC and MAC generated signals are based on TXC. Specified that RXC is derived from TXC to eliminate need for FIFOs in the MAC. d) Modified timing diagram to incorporate PC board load conditions. e) Removed references to SMII due to broad concerns about IP exclusivity and added specification for 10/100 MII operation. f) Modified Intellectual Property statement to address incorporation of IP from multiple sources. g) Modified document formatting.
1.2	Sept 11, 2000	a) Changed TD[4]/TXEN_TXERR signal name to TX_CTL b) Changed RD[4]/RXEN_RXERR signal name to RX_CTL c) Removed 100ps jitter requirement from TXC d) Changed RXC derivation to received data stream e) Clarified Table 1 description of TX_CTL and RX_CTL logical functions f) Required CRS assertion/deassertion to be synchronous for all speeds. g) Returned timing numbers to absolute from percentages. h) Relaxed 10/100 Duty cycle requirements to 40/60 i) Added verbage to allow clock cycle stretching during speed changes and receive data and clock acquistion. j) Modified Table 4 to incorporate optional in-band signaling of link status, speed, and duplex. k) Slight wording change on IP statements to limit scope and indemnify.

1.0 Purpose

The RGMII is intended to be an alternative to the IEEE802.3u MII, the IEEE802.3z GMII and the TBI. The principle objective is to reduce the number of pins required to interconnect the MAC and the PHY from a maximum of 28 pins (TBI) to 12 pins in a cost effective and technology independent manner. In order to accomplish this objective, the data paths and all associated control signals will be reduced and control signals will be multiplexed together and both edges of the clock will be used. For Gigabit operation, the clocks will operate at 125MHz, and for 10/100 operation, the clocks will operate at 2.5MHz or 25MHz respectively.

2.0 System Diagram

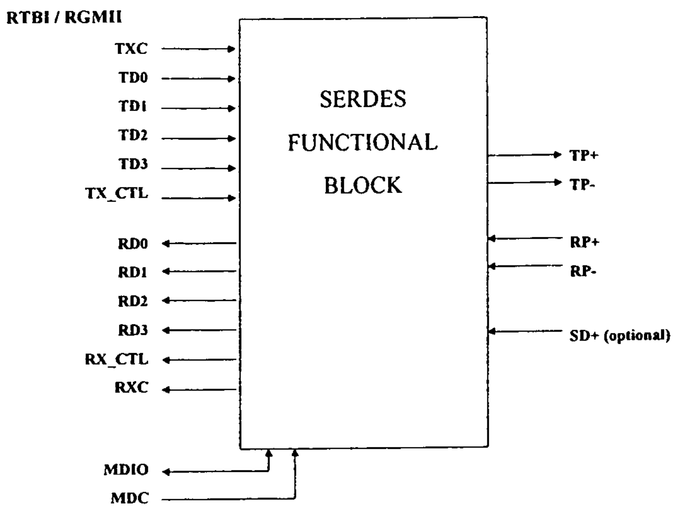

FIGURE 1 (System Diagram)

3.0 Signal Definitions

The RGMII will share four data path signals with the Reduced Ten Bit Interface (RTBI) and share control functionality with the fifth data signal. With the inclusion of the MDIO/MDC serial management signals, the RTBI will not require independent control signals like LK_REF, BYTE_EN, etc. Register assignment of SERDES control bits is left to the implementer.

Signal Name	RTBI	RGMII	Description
TXC	MAC	MAC	The transmit reference clock will be 125Mhz, 25Mhz, or 2.5Mhz +- 50ppm depending on speed.
TD[3:0]	PCS	MAC	In RTBI mode, contains bits 3:0 on ↑ of TXC and bits 8:5 on ↓ of TXC. In RGMII mode, bits 3:0 on ↑ of TXC, bits7:4 on ↓ of TXC
TX_CTL	PCS	MAC	In RTBI mode, contains the fifth bit on ↑ of TXC and tenth bit on ↓ of TXC. In RGMII mode, TXEN on ↑ of TXC, and a logical derivative of TXEN and TXERR on ↓ of TXC as described in section 3.4
RXC	PHY	PHY	The continuous receive reference clock will be 125Mhz, 25Mhz, or 2.5Mhz +- 50ppm. and shall be derived from the received data stream
RD[3:0]	PHY	PHY	In RTBI mode, contains bits 3:0 on ↑ of RXC and bits 8:5 on ↓ of RXC. In RGMII mode, bits 3:0 on ↑ of RXC, bits7:4 on ↓ of RXC
RX_CTL	PHY	PHY	In RTBI mode, contains the fifth bit on ↑ of RXC and tenth bit on ↓ of RXC. In RGMII mode, RXDV on ↑ of RXC, and a derivative of RXDV and RXERR on ↓ of RXC as described in section 3.4

TABLE 1 (Signal Definitions)

3.1 Signal Logic Conventions

All signals shall be conveyed with positive logic except as specified differently. For descriptive purposes, a signal shall be at a logic "high" when it is at a valid voltage level greater than V_{OH_MIN}, and logic "low" when it is at a valid voltage level less than V_{OL_MAX}.

3.2 Multiplexing of Data and Control

Multiplexing of data and control information is done by taking advantage of both edges of the reference clocks and sending the lower 4 bits on the ↑ edge and the upper 4 bits on the ↓ edge. Control signals can be multiplexed into a single clock cycle using the same technique.

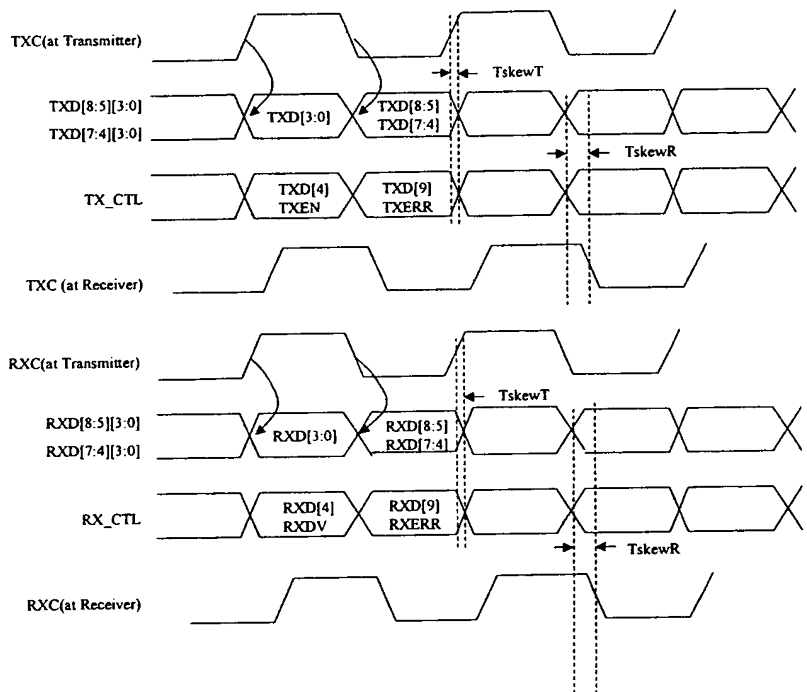

FIGURE 2 (Multiplexing & Timing Diagram)

3.3 Timing Specifics (Measured with the circuit shown in FIGURE 3 and a timing threshold voltage of 1.25v)

Timing for this interface will be such that the clock and data are generated simultaneously by the source of the signals and therefore skew between the clock and data is critical to proper operation. This approach is being used to provide tighter control of skew. Timing values are defined in percentages of the nominal clock period so to make this table speed independent.

Symbol	Parameter	Min	Typical	Max	Units
TskewT	Clock to Data output Skew (at Transmitter)	-500	0	500	ps
TskewR	Clock to Data input Skew (at Receiver) *note 1	1		2.8	ns
Tcyc	Clock Cycle Duration *note 2	7.2	8	8.8	ns
Duty_G	Duty Cycle for Gigabit *note 3	45	50	55	%
Duty_T	Duty Cycle for 10/100T *note 3	40	50	60	%
Tr / Tf	Rise / Fall Time (20-80%)			.75	ns

note 1: This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns will be added to the associated clock signal.

note 2: For 10Mbps and 100Mbps, Tcyc will scale to 400ns+-40ns and 40ns+-4ns respectively.

note 3: Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

TABLE 2

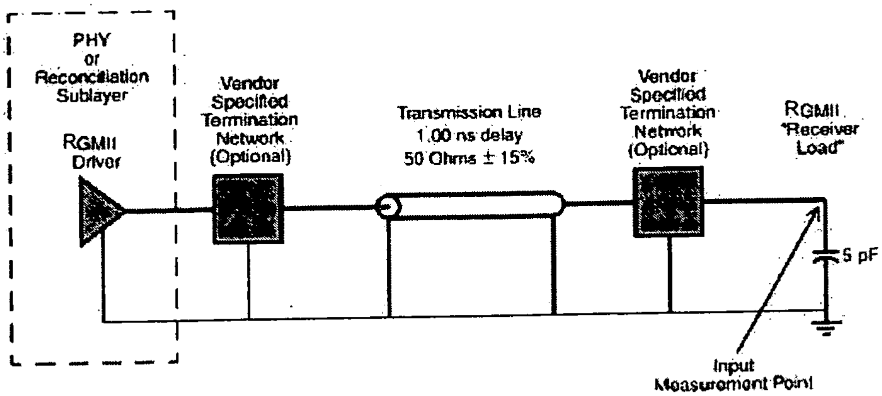

FIGURE 3

3.4 TXERR and RXERR Coding

To reduce power of this interface, TXERR and RXERR, will be encoded in a manner that minimizes transitions during normal network operation. This is done by the following encoding method. Note that the value of GMII_TX_ER and GMII_TX_EN are valid at the rising edge of the clock while TXERR is presented on the falling edge of the clock. RXERR coding behaves in the same way.

TXERR <= GMII_TX_ER (XOR) GMII_TX_EN
RXERR <= GMII_RX_ER (XOR) GMII_RX_DV

When receiving a valid frame with no errors, RXDV=true is generated as a logic high on the ↑ edge of RXC and RXERR=false is generated as a logic high the ↓ edge of RXC. When no frame is being received, RXDV=false is generated as a logic low on the ↑ edge of RXC and RXERR=false is generated as a logic low on the ↓ edge of RXC.

When receiving a valid frame with errors, RXDV=true is generated as logic high on the ↑ edge of RXC and RXERR=true is generated as a logic low on the ↓ edge of RXC.

TXERR is treated in a similar manner. During normal frame transmission, the signal stays at a logic high for both edges of TXC and during the period between frames where no errors are to be indicated, the signal stays low for both edges.

TX_CTL	GMII_TX_EN	GMII_TX_ER	TXD[7:0]	Description	PLS_DATA.request parameter
0,0	0	0	00 through FF	Normal inter-frame	TRANSMIT_COMPLETE
0,1	0	1	00 through 0E	Reserved —	
0,1	0	1	0F	Carrier Extend	EXTEND (eight bits)
0,1	0	1	10 through 1E	Reserved —	
0,1	0	1	1F	Carrier Extend Error	EXTEND_ERROR (eight bits)
0,1	0	1	20 through FE	Reserved —	
1,1	1	0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1,0	1	1	00 through FF	Transmit error propagation	No applicable parameter

NOTE—Values in TXD[7:0] column are in hexadecimal

TABLE 3 (Allowable Encoding of TXD, TXERR and TXEN)

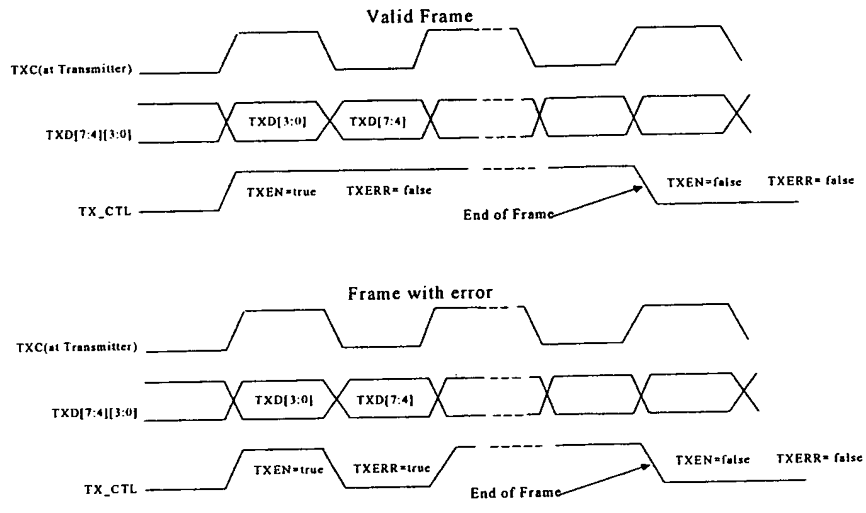

FIGURE 4

RX_CTL	GMII_RX_DV	GMII_RX_ER		RXD[7:0]	Description	PLS_DATA.indicate or PHY_ status parameter
0,0	0	0	#	xxx1 or xxx0	Normal inter-frame	Indicates link status 0=down, 1=up
0,0	0	0	#	x00x or x01x x10x or x11x	Normal inter-frame	Indicates RXC clock speed 00=2.5Mhz, 01=25Mhz, and 10=125Mhz, 11=reserved
0,0	0	0	#	1xxx or 0xxx	Normal inter-frame	Indicates duplex status 0=half-duplex, 1=full duplex
0,1	0	1	*	00	Reserved	—
0,1	0	1	*	01through 0D	Reserved	—
0,1	0	1	*	0E	False Carrier indication	False Carrier Present
0,1	0	1	*	0F	Carrier Extend	EXTEND (eight bits)
0,1	0	1	*	10 through 1E	Reserved	—
0,1	0	1	*	1F	Carrier Extend Error	ZERO, ONE (eight bits)
0,1	0	1	*	20 through FE	Reserved	—
0,1	0	1	*	FF	Carrier Sense	PLS_Carrier.Indicate
1,1	1	0	*	00 through FF	Normal data reception	ZERO, ONE (eight bits)
1,0	1	1	*	00 through FF	Data reception error	ZERO, ONE(eight bits)

* NOTE— (Required Function) Values in RXD[7:0] column are in hexadecimal.
# NOTE— (Optional) Values in RXD[7:0] column are in binary; nibbles are repeated on ↑ edge and ↓ edge.

TABLE 4 (Allowable Encoding of RXD, RXDV and RXERR)

3.4.1 In-Band Status (Optional)

In order to ease detection of the link status, speed and duplex mode of the PHY, inter-frame signals will be placed onto the RXD[3:0] signals as indicated in table 4. The status of the PHY shall be indicated whenever Normal Data, Data Error, Carrier Extend, Carrier Sense, or False Carrier are not present. When link status is down, PHY speed and duplex are defined by the PHY's internal setting.

3.4.2 In-Band Status (Required)

In half duplex mode, CRS is indicated by the case where RXDV is true, or the case where RXDV is false, RXERR is true, and a value of FF exists on the RXD[7:0] bits simultaneously or in the case where a Carrier Extend, Carrier Extend Error or False Carrier are occurring as defined in Table 4. Carrier Extend and Carrier Extend Error are applicable to Gigabit speeds only.

Collision is determined at the MAC by the assertion of TXEN being true while either CRS or RXDV are true. The PHY will not assert CRS as a result of TXEN being true.

4.0 Electrical Characteristics

The RGMII and RTBI signals will be based upon 2.5v CMOS interface voltages as defined by JEDEC EIA/JESD8-5.

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -1.0mA; V_{CC} = Min	2.0	VDD+.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.0mA; V_{CC}=Min	GND-.3	0.40	V
V_{IH}	Input High Voltage	V_{IH} > V_{IH}_Min; V_{CC}=Min	1.7	-	V
V_{IL}	Input Low Voltage	V_{IH} > V_{IL}_Max; V_{CC}=Min	-	.70	V
I_{IH}	Input High Current	V_{CC} = Max; V_{IN} = 2.5V	-	15	uA
I_{IL}	Input Low Current	V_{CC} = Max; V_{IN} = 0.4V	-15	-	uA

TABLE 5

5.0 10/100 Functionality

This interface can be used to implement the 10/100 Mbps Ethernet Media Independent Interface (MII) by reducing the clock rate to 25MHz for 100Mbps operation and 2.5MHz for 10Mbps. The TXC will always be generated by the MAC and RXC will be generated by the PHY. During packet reception, the RXC may be stretched on either the positive or negative pulse to accommodate the transition from the free running clock to a data-synchronous clock domain. When the speed of the PHY changes, a similar stretching of the positive or negative pulses is allowed. No glitching of the clocks are allowed during speed transitions.

This interface will operate at 10 and 100Mbps speeds exactly the same way it does at Gigabit speed with the exception that the data may be duplicated on the ↓ edge of the appropriate clock.

The MAC will hold TX_CTL low until it has ensured that it is operating at the same speed as the PHY.

6.0 Mode Selection

The decision about which mode of operation this interface will use is left to the implementers. It may be done with hard-wired pins, or through register bits that are controlled by software.

7.0 Hewlett Packard Intellectual Property

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7.1 Contributions of Intellectual Property

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7.2 Disclaimer

This RGMII Specification is provided "as is" with no warranties whatsoever, including any warranty of merchantability, non-infringement, fitness for any particular purpose, or any warranty otherwise arising out of any proposal, specification, or sample.

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Reduced Gigabit Media Independent Interface (RGMII)

9/22/2000
Version 1.2a

Reduced Pin-count Interface
For
Gigabit Ethernet Physical Layer Devices

Preliminary Draft for review only

Exhibit 12

Revision Level	Date	Revision Description
1.0	June 1, 2000	Released for public review and comment
1.1	August 1, 2000	a) Modified RXERR and TXERR coding to reduce transitions and power in normal conditions. b) Removed CRS_COL pin and incorporated coding alternative for half duplex implementation. c) Found and corrected some inconsistencies in which clock was specified for timing. PHY generated signals are based on RXC and MAC generated signals are based on TXC. Specified that RXC is derived from TXC to eliminate need for FIFOs in the MAC. d) Modified timing diagram to incorporate PC board load conditions. e) Removed references to SMII due to broad concerns about IP exclusivity and added specification for 10/100 MII operation. f) Modified Intellectual Property statement to address incorporation of IP from multiple sources. g) Modified document formatting.
1.2	Sept 11, 2000	a) Changed TD[4]/TXEN_TXERR signal name to TX_CTL b) Changed RD[4]/RXEN_RXERR signal name to RX_CTL c) Removed 100ps jitter requirement from TXC d) Changed RXC derivation to received data stream e) Clarified Table 1 description of TX_CTL and RX_CTL logical functions f) Required CRS assertion/deassertion to be synchronous for all speeds. g) Returned timing numbers to absolute from percentages. h) Relaxed 10/100 Duty cycle requirements to 40/60 i) Added verbage to allow clock cycle stretching during speed changes and receive data and clock acquistion. j) Modified Table 4 to incorporate optional in-band signaling of link status, speed, and duplex. k) Slight wording change on IP statements to limit scope and indemnify.
1.2a	Sept 22, 2000	a) Clarified 3.4.2 statement to eliminate suggestion that in-band status was only required for half-duplex. b) Modified Table 2 to from "Clock to Data skew" to "Data to Clock skew" to clarify the fact that clock is delayed relative to data. c) Modified section 4.0 to clarify that MDIO/MDC are also operating at 2.5v CMOS levels.

1.0 Purpose

The RGMII is intended to be an alternative to the IEEE802.3u MII, the IEEE802.3z GMII and the TBI. The principle objective is to reduce the number of pins required to interconnect the MAC and the PHY from a maximum of 28 pins (TBI) to 12 pins in a cost effective and technology independent manner. In order to accomplish this objective, the data paths and all associated control signals will be reduced and control signals will be multiplexed together and both edges of the clock will be used. For Gigabit operation, the clocks will operate at 125MHz, and for 10/100 operation, the clocks will operate at 2.5MHz or 25MHz respectively.

2.0 System Diagram

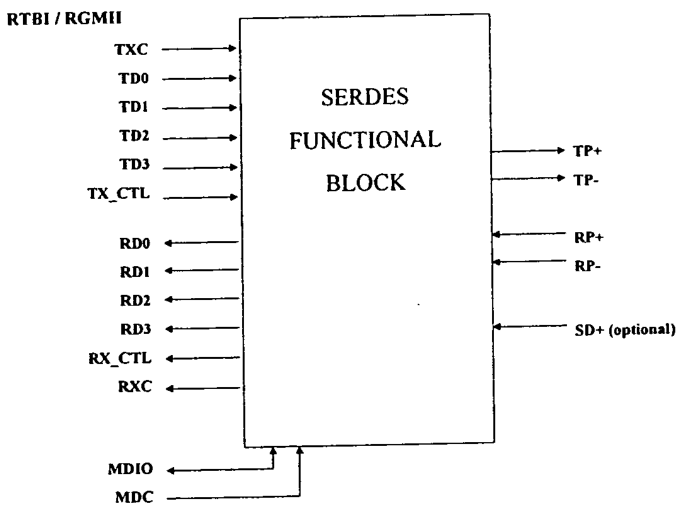

FIGURE 1 (System Diagram)

3.0 Signal Definitions

The RGMII will share four data path signals with the Reduced Ten Bit Interface (RTBI) and share control functionality with the fifth data signal. With the inclusion of the MDIO/MDC serial management signals, the RTBI will not require independent control signals like LK_REF, BYTE_EN, etc. Register assignment of SERDES control bits is left to the implementer.

Signal Name	RTBI	RGMII	Description
TXC	MAC	MAC	The transmit reference clock will be 125Mhz, 25Mhz, or 2.5Mhz +- 50ppm depending on speed.
TD[3:0]	PCS	MAC	In RTBI mode, contains bits 3:0 on ↑ of TXC and bits 8:5 on ↓ of TXC. In RGMII mode, bits 3:0 on ↑ of TXC, bits7:4 on ↓ of TXC
TX_CTL	PCS	MAC	In RTBI mode, contains the fifth bit on ↑ of TXC and tenth bit on ↓ of TXC. In RGMII mode, TXEN on ↑ of TXC, and a logical derivative of TXEN and TXERR on ↓ of TXC as described in section 3.4
RXC	PHY	PHY	The continuous receive reference clock will be 125Mhz, 25Mhz, or 2.5Mhz +- 50ppm. and shall be derived from the received data stream
RD[3:0]	PHY	PHY	In RTBI mode, contains bits 3:0 on ↑ of RXC and bits 8:5 on ↓ of RXC. In RGMII mode, bits 3:0 on ↑ of RXC, bits7:4 on ↓ of RXC
RX_CTL	PHY	PHY	In RTBI mode, contains the fifth bit on ↑ of RXC and tenth bit on ↓ of RXC. In RGMII mode, RXDV on ↑ of RXC, and a derivative of RXDV and RXERR on ↓ of RXC as described in section 3.4

TABLE 1 (Signal Definitions)

3.1 Signal Logic Conventions

All signals shall be conveyed with positive logic except as specified differently. For descriptive purposes, a signal shall be at a logic "high" when it is at a valid voltage level greater than VOH_MIN, and logic "low" when it is at a valid voltage level less than VOL_MAX.

3.2 Multiplexing of Data and Control

Multiplexing of data and control information is done by taking advantage of both edges of the reference clocks and sending the lower 4 bits on the ↑ edge and the upper 4 bits on the ↓ edge. Control signals can be multiplexed into a single clock cycle using the same technique.

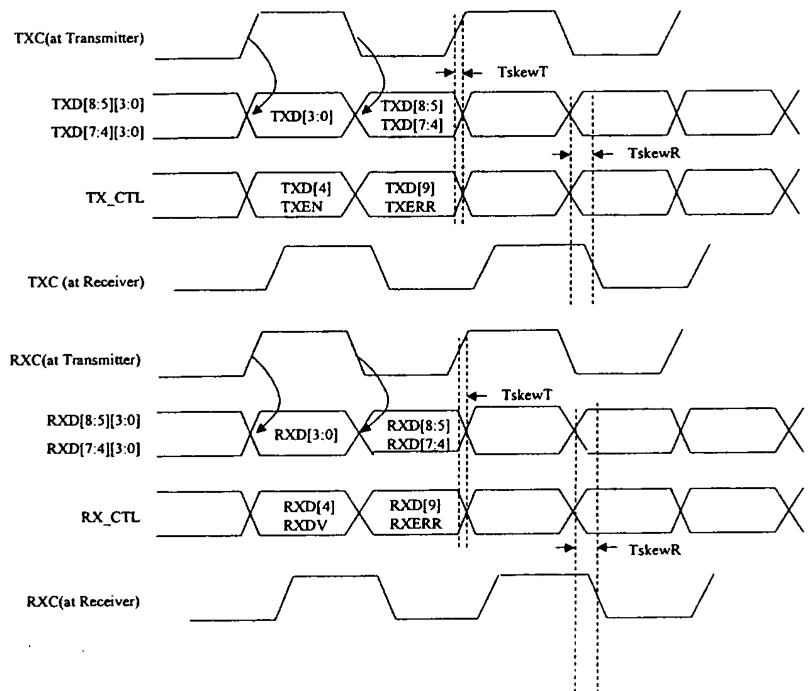

FIGURE 2 (Multiplexing & Timing Diagram)

3.3 Timing Specifics (Measured with the circuit shown in FIGURE 3 and a timing threshold voltage of 1.25v)

Timing for this interface will be such that the clock and data are generated simultaneously by the source of the signals and therefore skew between the clock and data is critical to proper operation. This approach is being used to provide tighter control of skew. Timing values are defined in percentages of the nominal clock period so to make this table speed independent.

Symbol	Parameter	Min	Typical	Max	Units
TskewT	Data to Clock output Skew (at Transmitter)	-500	0	500	ps
TskewR	Data to Clock input Skew (at Receiver) *note 1	1		2.8	ns
Tcyc	Clock Cycle Duration *note 2	7.2	8	8.8	ns
Duty_G	Duty Cycle for Gigabit *note 3	45	50	55	%
Duty_T	Duty Cycle for 10/100T *note 3	40	50	60	%
Tr / Tf	Rise / Fall Time (20-80%)			.75	ns

note 1: This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns will be added to the associated clock signal.

note 2: For 10Mbps and 100Mbps, Tcyc will scale to 400ns+-40ns and 40ns+-4ns respectively.

note 3: Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

TABLE 2

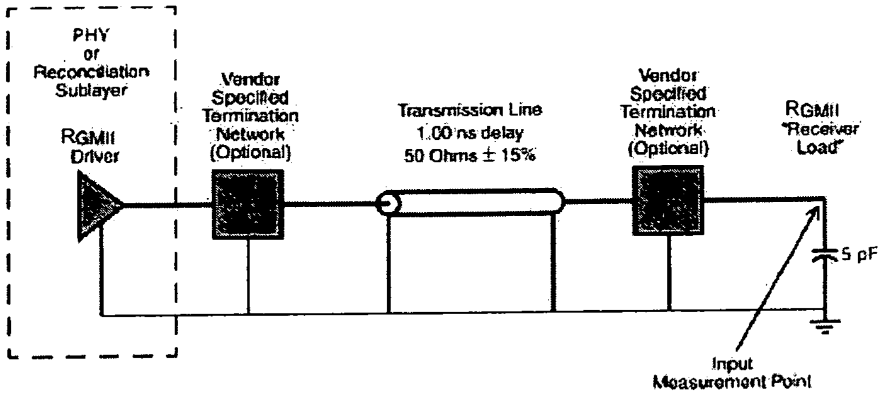

FIGURE 3

3.4 TXERR and RXERR Coding

To reduce power of this interface, TXERR and RXERR, will be encoded in a manner that minimizes transitions during normal network operation. This is done by the following encoding method. Note that the value of GMII_TX_ER and GMII_TX_EN are valid at the rising edge of the clock while TXERR is presented on the falling edge of the clock. RXERR coding behaves in the same way.

TXERR <= GMII_TX_ER (XOR) GMII_TX_EN
RXERR <= GMII_RX_ER (XOR) GMII_RX_DV

When receiving a valid frame with no errors, RXDV=true is generated as a logic high on the ↑ edge of RXC and RXERR=false is generated as a logic high the ↓ edge of RXC. When no frame is being received, RXDV=false is generated as a logic low on the ↑ edge of RXC and RXERR=false is generated as a logic low on the ↓ edge of RXC.

When receiving a valid frame with errors, RXDV=true is generated as logic high on the ↑ edge of RXC and RXERR=true is generated as a logic low on the ↓ edge of RXC.

TXERR is treated in a similar manner. During normal frame transmission, the signal stays at a logic high for both edges of TXC and during the period between frames where no errors are to be indicated, the signal stays low for both edges.

TX_CTL	GMII_TX_EN	GMII_TX_ER	TXD[7:0]	Description	PLS_DATA.request parameter
0,0	0	0	00 through FF	Normal inter-frame	TRANSMIT_COMPLETE
0,1	0	1	00 through 0E	Reserved —	
0,1	0	1	0F	Carrier Extend	EXTEND (eight bits)
0,1	0	1	10 through 1E	Reserved —	
0,1	0	1	1F	Carrier Extend Error	EXTEND_ERROR (eight bits)
0,1	0	1	20 through FE	Reserved —	
1,1	1	0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1,0	1	1	00 through FF	Transmit error propagation	No applicable parameter

NOTE—Values in TXD[7:0] column are in hexadecimal

TABLE 3 (Allowable Encoding of TXD, TXERR and TXEN)

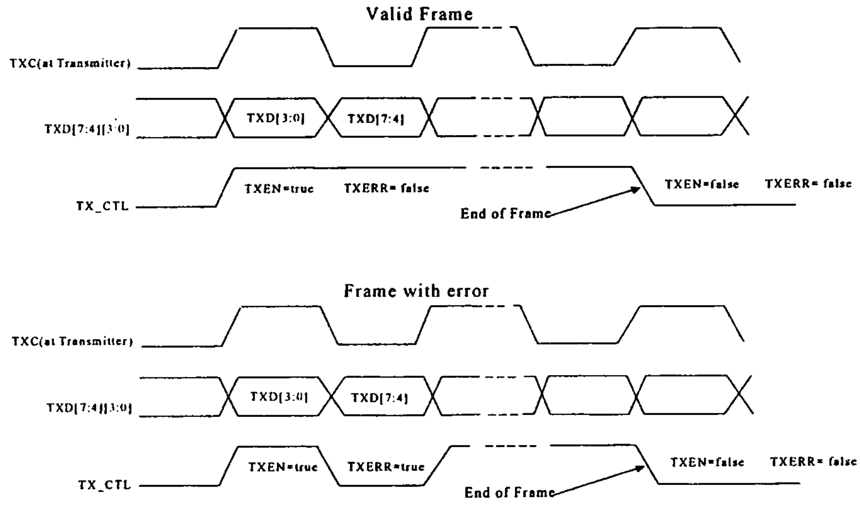

FIGURE 4

RX_CTL	GMII_RX_DV	GMII_RX_ER		RXD[7:0]	Description	PLS_DATA.indicate or PHY_ status parameter
0,0	0	0	#	xxx1 or xxx0	Normal inter-frame	Indicates link status 0=down, 1=up
0,0	0	0	#	x00x or x01x x10x or x11x	Normal inter-frame	Indicates RXC clock speed 00=2.5Mhz, 01=25Mhz, and 10=125Mhz, 11=reserved
0,0	0	0	#	1xxx or 0xxx	Normal inter-frame	Indicates duplex status 0=half-duplex, 1=full duplex
0,1	0	1	*	00	Reserved	—
0,1	0	1	*	01through 0D	Reserved	—
0,1	0	1	*	0E	False Carrier indication	False Carrier Present
0,1	0	1	*	0F	Carrier Extend	EXTEND (eight bits)
0,1	0	1	*	10 through 1E	Reserved	—
0,1	0	1	*	1F	Carrier Extend Error	ZERO, ONE (eight bits)
0,1	0	1	*	20 through FE	Reserved	—
0,1	0	1	*	FF	Carrier Sense	PLS_Carrier.Indicate
1,1	1	0	*	00 through FF	Normal data reception	ZERO, ONE (eight bits)
1,0	1	1	*	00 through FF	Data reception error	ZERO, ONE(eight bits)

• NOTE— (Required Function) Values in RXD[7:0] column are in hexadecimal.
NOTE— (Optional) Values in RXD[7:0] column are in binary; nibbles are repeated on ↑ edge and ↓ edge.

TABLE 4 (Allowable Encoding of RXD, RXDV and RXERR)

3.4.1 In-Band Status (Optional)

In order to ease detection of the link status, speed and duplex mode of the PHY, inter-frame signals will be placed onto the RXD[3:0] signals as indicated in table 4. The status of the PHY shall be indicated whenever Normal Data, Data Error, Carrier Extend, Carrier Sense, or False Carrier are not present. When link status is down, PHY speed and duplex are defined by the PHY's internal setting.

3.4.2 In-Band Status (Required)

CRS is indicated by the case where RXDV is true, or the case where RXDV is false, RXERR is true, and a value of FF exists on the RXD[7:0] bits simultaneously or in the case where a Carrier Extend, Carrier Extend Error or False Carrier are occurring as defined in Table 4. Carrier Extend and Carrier Extend Error are applicable to Gigabit speeds only.

Collision is determined at the MAC by the assertion of TXEN being true while either CRS or RXDV are true. The PHY will not assert CRS as a result of TXEN being true.

4.0 Electrical Characteristics

The RGMII and RTBI signals (including MDIO/MDC) will be based upon 2.5v CMOS interface voltages as defined by JEDEC EIA/JESD8-5.

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -1.0mA; V_{CC} = Min	2.0	VDD+.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.0mA; V_{CC}=Min	GND-.3	0.40	V
V_{IH}	Input High Voltage	V_{IH} > V_{IH}_Min; V_{CC}=Min	1.7	-	V
V_{IL}	Input Low Voltage	V_{IH} > V_{IL}_Max; V_{CC}=Min	-	.70	V
I_{IH}	Input High Current	V_{CC} = Max; V_{IN} = 2.5V	-	15	uA
I_{IL}	Input Low Current	V_{CC} = Max; V_{IN} = 0.4V	-15	-	uA

TABLE 5

5.0 10/100 Functionality

This interface can be used to implement the 10/100 Mbps Ethernet Media Independent Interface (MII) by reducing the clock rate to 25MHz for 100Mbps operation and 2.5MHz for 10Mbps. The TXC will always be generated by the MAC and RXC will be generated by the PHY. During packet reception, the RXC may be stretched on either the positive or negative pulse to accommodate the transition from the free running clock to a data-synchronous clock domain. When the speed of the PHY changes, a similar stretching of the positive or negative pulses is allowed. No glitching of the clocks are allowed during speed transitions.

This interface will operate at 10 and 100Mbps speeds exactly the same way it does at Gigabit speed with the exception that the data may be duplicated on the ↓ edge of the appropriate clock.

The MAC will hold TX_CTL low until it has ensured that it is operating at the same speed as the PHY.

6.0 Mode Selection

The decision about which mode of operation this interface will use is left to the implementers. It may be done with hard-wired pins, or through register bits that are controlled by software.

7.0 Hewlett Packard Intellectual Property

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Reduced Gigabit Media Independent Interface (RGMII)

12/10/2000
Version 1.3

Reduced Pin-count Interface
For
Gigabit Ethernet Physical Layer Devices

Preliminary Draft for review only

Exhibit 13

Revision Level	Date	Revision Description
1.0	June 1, 2000	Released for public review and comment
1.1	August 1, 2000	a) Modified RXERR and TXERR coding to reduce transitions and power in normal conditions. b) Removed CRS_COL pin and incorporated coding alternative for half duplex implementation. c) Found and corrected some inconsistencies in which clock was specified for timing. PHY generated signals are based on RXC and MAC generated signals are based on TXC. Specified that RXC is derived from TXC to eliminate need for FIFOs in the MAC. d) Modified timing diagram to incorporate PC board load conditions. e) Removed references to SMII due to broad concerns about IP exclusivity and added specification for 10/100 MII operation. f) Modified Intellectual Property statement to address incorporation of IP from multiple sources. g) Modified document formatting.
1.2	Sept 11, 2000	a) Changed TD[4]/TXEN_TXERR signal name to TX_CTL b) Changed RD[4]/RXEN_RXERR signal name to RX_CTL c) Removed 100ps jitter requirement from TXC d) Changed RXC derivation to received data stream e) Clarified Table 1 description of TX_CTL and RX_CTL logical functions f) Required CRS assertion/deassertion to be synchronous for all speeds. g) Returned timing numbers to absolute from percentages. h) Relaxed 10/100 Duty cycle requirements to 40/60 i) Added verbage to allow clock cycle stretching during speed changes and receive data and clock acquistion. j) Modified Table 4 to incorporate optional in-band signaling of link status, speed, and duplex. k) Slight wording change on IP statements to limit scope and indemnify.
1.2a	Sept 22, 2000	a) Clarified 3.4.2 statement to eliminate suggestion that in-band status was only required for half-duplex. b) Modified Table 2 to from "Clock to Data skew" to "Data to Clock skew" to clarify the fact that clock is delayed relative to data. c) Modified section 4.0 to clarify that MDIO/MDC are also operating at 2.5v CMOS levels.
1.3	Dec 10, 2000	a) Clarified RX_CTL and TX_CTL functionality by modifying Figure 4 and adding Figure 5 and Figure 6. b) Modified Table 3 to include the value of FF as reserved when TX_CTL=0,1. c) Reduced TskewR in Table 2 to a value of 2.6ns maximum for Gigabit operation and relaxed it in note #1 for 10/100 operation. d) Put maximum delay in note #1 of Table 2 of 2ns to ensure minimum setup time for subsequent edges.

1.0 Purpose

The RGMII is intended to be an alternative to the IEEE802.3u MII, the IEEE802.3z GMII and the TBI. The principle objective is to reduce the number of pins required to interconnect the MAC and the PHY from a maximum of 28 pins (TBI) to 12 pins in a cost effective and technology independent manner. In order to accomplish this objective, the data paths and all associated control signals will be reduced and control signals will be multiplexed together and both edges of the clock will be used. For Gigabit operation, the clocks will operate at 125MHz, and for 10/100 operation, the clocks will operate at 2.5MHz or 25MHz respectively.

2.0 System Diagram

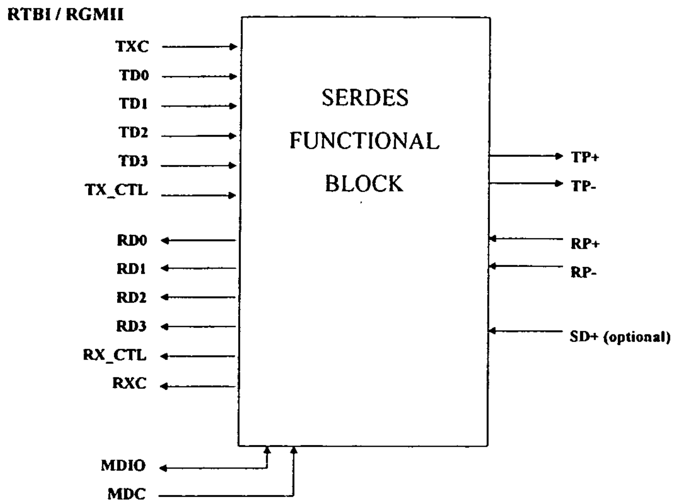

FIGURE 1 (System Diagram)

3.0 Signal Definitions

The RGMII will share four data path signals with the Reduced Ten Bit Interface (RTBI) and share control functionality with the fifth data signal. With the inclusion of the MDIO/MDC serial management signals, the RTBI will not require independent control signals like LK_REF, BYTE_EN, etc. Register assignment of SERDES control bits is left to the implementer.

Signal Name	RTBI	RGMII	Description
TXC	MAC	MAC	The transmit reference clock will be 125Mhz, 25Mhz, or 2.5Mhz +- 50ppm depending on speed.
TD[3:0]	PCS	MAC	In RTBI mode, contains bits 3:0 on ↑ of TXC and bits 8:5 on ↓ of TXC. In RGMII mode, bits 3:0 on ↑ of TXC, bits7:4 on ↓ of TXC
TX_CTL	PCS	MAC	In RTBI mode, contains the fifth bit on ↑ of TXC and tenth bit on ↓ of TXC. In RGMII mode, TXEN on ↑ of TXC, and a logical derivative of TXEN and TXERR on ↓ of TXC as described in section 3.4
RXC	PHY	PHY	The continuous receive reference clock will be 125Mhz, 25Mhz, or 2.5Mhz +- 50ppm. and shall be derived from the received data stream
RD[3:0]	PHY	PHY	In RTBI mode, contains bits 3:0 on ↑ of RXC and bits 8:5 on ↓ of RXC. In RGMII mode, bits 3:0 on ↑ of RXC, bits7:4 on ↓ of RXC
RX_CTL	PHY	PHY	In RTBI mode, contains the fifth bit on ↑ of RXC and tenth bit on ↓ of RXC. In RGMII mode, RXDV on ↑ of RXC, and a derivative of RXDV and RXERR on ↓ of RXC as described in section 3.4

TABLE 1 (Signal Definitions)

3.1 Signal Logic Conventions

All signals shall be conveyed with positive logic except as specified differently. For descriptive purposes, a signal shall be at a logic "high" when it is at a valid voltage level greater than V_{OH_MIN}, and logic "low" when it is at a valid voltage level less than V_{OL_MAX}.

3.2 Multiplexing of Data and Control

Multiplexing of data and control information is done by taking advantage of both edges of the reference clocks and sending the lower 4 bits on the ↑ edge and the upper 4 bits on the ↓ edge. Control signals can be multiplexed into a single clock cycle using the same technique.

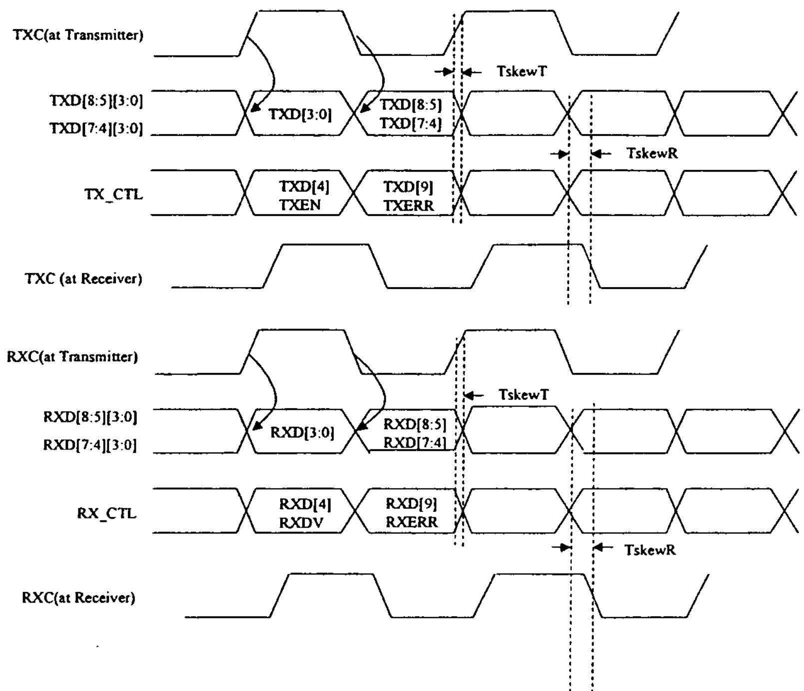

FIGURE 2 (Multiplexing & Timing Diagram)

3.3 Timing Specifics (Measured with the circuit shown in FIGURE 3 and a timing threshold voltage of 1.25v)

Timing for this interface will be such that the clock and data are generated simultaneously by the source of the signals and therefore skew between the clock and data is critical to proper operation. This approach is being used to provide tighter control of skew. Timing values are defined in percentages of the nominal clock period so to make this table speed independent.

Symbol	Parameter	Min	Typical	Max	Units
TskewT	Data to Clock output Skew (at Transmitter)	-500	0	500	ps
TskewR	Data to Clock input Skew (at Receiver) *note 1	1		2.6	ns
Tcyc	Clock Cycle Duration *note 2	7.2	8	8.8	ns
Duty_G	Duty Cycle for Gigabit *note 3	45	50	55	%
Duty_T	Duty Cycle for 10/100T *note 3	40	50	60	%
Tr / Tf	Rise / Fall Time (20-80%)			.75	ns

note 1: This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns and less than 2.0ns will be added to the associated clock signal. For 10/100 the Max value is unspecified.

note 2: For 10Mbps and 100Mbps, Tcyc will scale to 400ns+-40ns and 40ns+-4ns respectively.

note 3: Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

TABLE 2

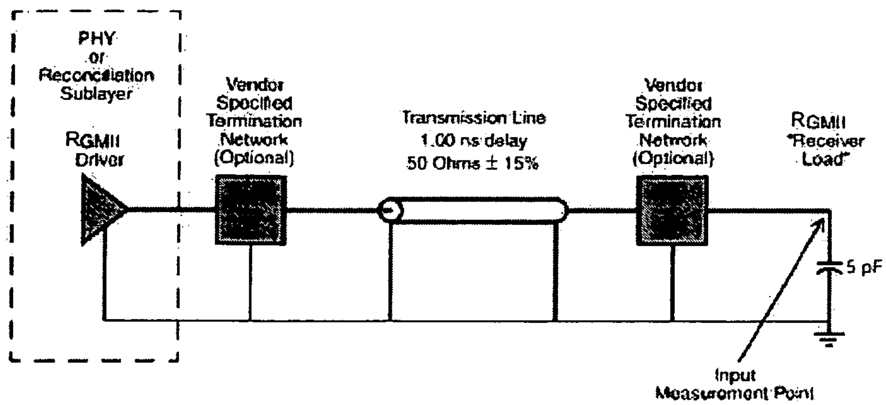

FIGURE 3

3.4 TXERR and RXERR Coding

To reduce power of this interface, TXERR and RXERR, will be encoded in a manner that minimizes transitions during normal network operation. This is done by the following encoding method. Note that the value of GMII_TX_ER and GMII_TX_EN are valid at the rising edge of the clock while TXERR is presented on the falling edge of the clock. RXERR coding behaves in the same way.

TXERR <= GMII_TX_ER (XOR) GMII_TX_EN
RXERR <= GMII_RX_ER (XOR) GMII_RX_DV

When receiving a valid frame with no errors, RXDV=true is generated as a logic high on the ↑ edge of RXC and RXERR=false is generated as a logic high the ↓ edge of RXC. When no frame is being received, RXDV=false is generated as a logic low on the ↑ edge of RXC and RXERR=false is generated as a logic low on the ↓ edge of RXC.

When receiving a valid frame with errors, RXDV=true is generated as logic high on the ↑ edge of RXC and RXERR=true is generated as a logic low on the ↓ edge of RXC.

TXERR is treated in a similar manner. During normal frame transmission, the signal stays at a logic high for both edges of TXC and during the period between frames where no errors are to be indicated, the signal stays low for both edges.

TX_CTL	GMII_TX_EN	GMII_TX_ER	TXD[7:0]	Description	PLS_DATA.request parameter
0,0	0	0	00 through FF	Normal inter-frame	TRANSMIT_COMPLETE
0,1	0	1	00 through 0E	Reserved —	
0,1	0	1	0F	Carrier Extend	EXTEND (eight bits)
0,1	0	1	10 through 1E	Reserved —	
0,1	0	1	1F	Carrier Extend Error	EXTEND_ERROR (eight bits)
0,1	0	1	20 through FF	Reserved —	
1,1	1	0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1,0	1	1	00 through FF	Transmit error propagation	No applicable parameter

NOTE—Values in TXD[7:0] column are in hexadecimal

TABLE 3 (Allowable Encoding of TXD, TXERR and TXEN)

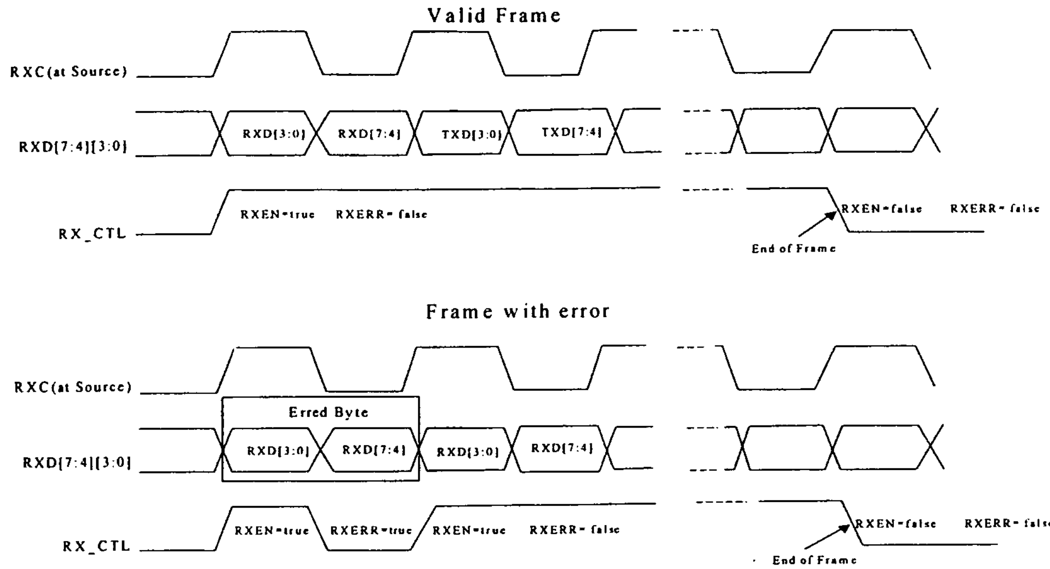

FIGURE 4

RX_CTL	GMII_RX_DV	GMII_RX_ER		RXD[7:0]	Description	PLS_DATA.indicate or PHY_ status parameter
0,0	0	0	#	xxx1 or xxx0	Normal inter-frame	Indicates link status 0=down, 1=up
0,0	0	0	#	x00x or x01x x10x or x11x	Normal inter-frame	Indicates RXC clock speed 00=2.5Mhz, 01=25Mhz, and 10=125Mhz, 11=reserved
0,0	0	0	#	1xxx or 0xxx	Normal inter-frame	Indicates duplex status 0=half-duplex, 1=full duplex
0,1	0	1	*	00	Reserved	—
0,1	0	1	*	01through 0D	Reserved	—
0,1	0	1	*	0E	False Carrier indication	False Carrier Present
0,1	0	1	*	0F	Carrier Extend	EXTEND (eight bits)
0,1	0	1	*	10 through 1E	Reserved	—
0,1	0	1	*	1F	Carrier Extend Error	ZERO, ONE (eight bits)
0,1	0	1	*	20 through FE	Reserved	—
0,1	0	1	*	FF	Carrier Sense	PLS_Carrier.Indicate
1,1	1	0	*	00 through FF	Normal data reception	ZERO, ONE (eight bits)
1,0	1	1	*	00 through FF	Data reception error	ZERO, ONE(eight bits)

* NOTE— (Required Function) Values in RXD[7:0] column are in hexadecimal.
# NOTE— (Optional) Values in RXD[7:0] column are in binary; nibbles are repeated on ↑ edge and ↓ edge.

TABLE 4 (Allowable Encoding of RXD, RXDV and RXERR)

3.4.1 In-Band Status (Optional)

In order to ease detection of the link status, speed and duplex mode of the PHY, inter-frame signals will be placed onto the RXD[3:0] signals as indicated in table 4. The status of the PHY shall be indicated whenever Normal Data, Data Error, Carrier Extend, Carrier Sense, or False Carrier are not present. When link status is down, PHY speed and duplex are defined by the PHY's internal setting.

3.4.2 In-Band Status (Required)

CRS is indicated by the case where RXDV is true, or the case where RXDV is false, RXERR is true, and a value of FF exists on the RXD[7:0] bits simultaneously or in the case where a Carrier Extend, Carrier Extend Error or False Carrier are occurring as defined in Table 4. Carrier Extend and Carrier Extend Error are applicable to Gigabit speeds only.

Collision is determined at the MAC by the assertion of TXEN being true while either CRS or RXDV are true. The PHY will not assert CRS as a result of TXEN being true.

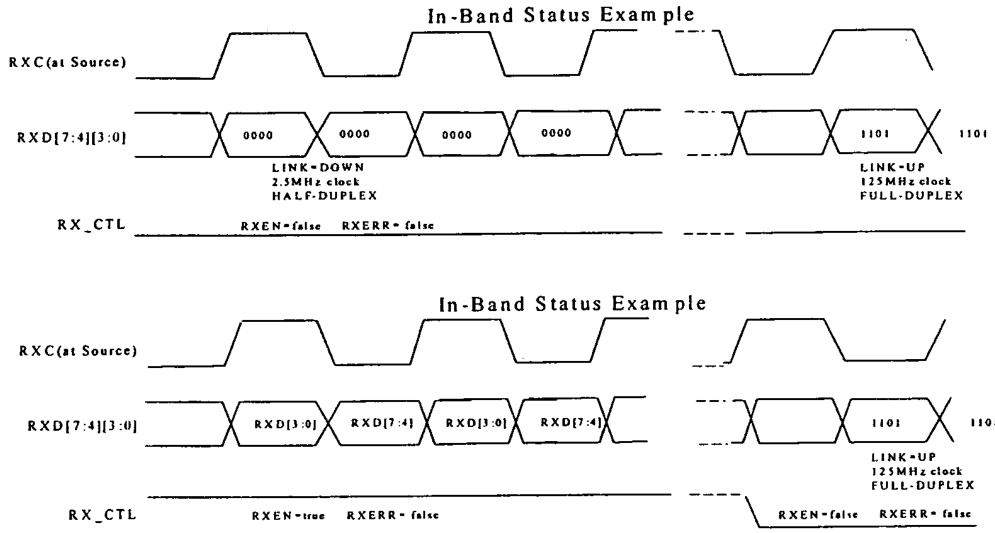

FIGURE 5

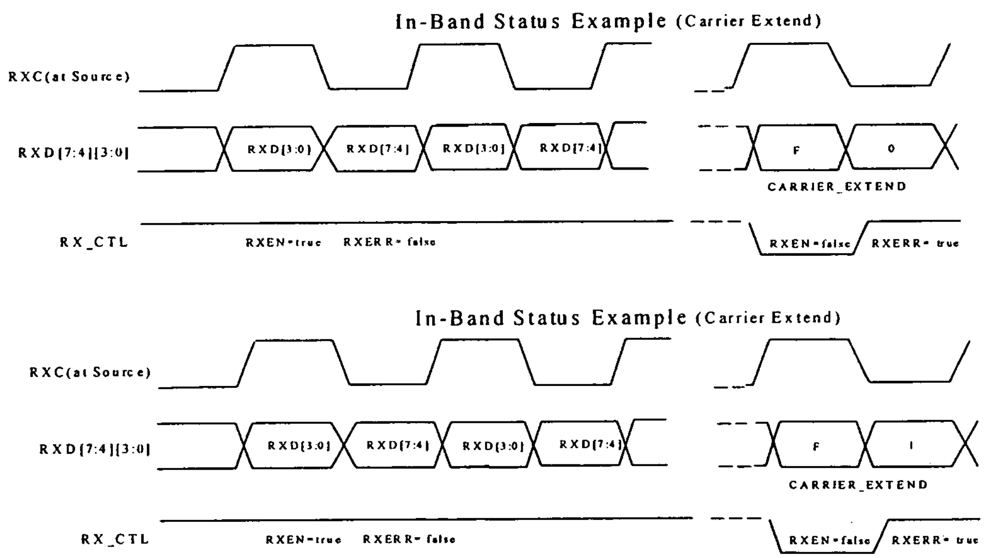

FIGURE 6

4.0 Electrical Characteristics

The RGMII and RTBI signals (including MDIO/MDC) will be based upon 2.5v CMOS interface voltages as defined by JEDEC EIA/JESD8-5.

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -1.0mA; V_{CC} = Min	2.0	VDD+.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.0mA; V_{CC}=Min	GND-.3	0.40	V
V_{IH}	Input High Voltage	V_{IH} > V_{IH}_Min; V_{CC}=Min	1.7	–	V
V_{IL}	Input Low Voltage	V_{IH} > V_{IL}_Max; V_{CC}=Min	-	.70	V
I_{IH}	Input High Current	V_{CC} = Max; V_{IN} = 2.5V	-	15	uA
I_{IL}	Input Low Current	V_{CC} = Max; V_{IN} = 0.4V	-15	-	uA

TABLE 5

5.0 10/100 Functionality

This interface can be used to implement the 10/100 Mbps Ethernet Media Independent Interface (MII) by reducing the clock rate to 25MHz for 100Mbps operation and 2.5MHz for 10Mbps. The TXC will always be generated by the MAC and RXC will be generated by the PHY. During packet reception, the RXC may be stretched on either the positive or negative pulse to accommodate the transition from the free running clock to a data-synchronous clock domain. When the speed of the PHY changes, a similar stretching of the positive or negative pulses is allowed. No glitching of the clocks are allowed during speed transitions.

This interface will operate at 10 and 100Mbps speeds exactly the same way it does at Gigabit speed with the exception that the data may be duplicated on the ↓ edge of the appropriate clock.

The MAC will hold TX_CTL low until it has ensured that it is operating at the same speed as the PHY.

6.0 Mode Selection

The decision about which mode of operation this interface will use is left to the implementers. It may be done with hard-wired pins, or through register bits that are controlled by software.

7.0 Hewlett Packard Intellectual Property

The Hewlett-Packard Company has released its proprietary rights to information contained in this document for the express purpose of implementation of this specification to encourage others to adopt this interface as an industry standard. Any company wishing to use this specification may do so if they will in turn relinquish their proprietary rights to information contained or referenced herein. Any questions concerning this release should be directed to the Director of Intellectual Property, Hewlett-Packard Company, 3000 Hanover Street, Palo Alto, CA.

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7.2 Disclaimer

This RGMII Specification is provided "as is" with no warranties whatsoever, including any warranty of merchantability, non-infringement, fitness for any particular purpose, or any warranty otherwise arising out of any proposal, specification, or sample.

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Reduced Gigabit Media Independent Interface (RGMII)

4/1/2002
Version 2.0

Reduced Pin-count Interface
For
Gigabit Ethernet Physical Layer Devices

Exhibit 14

Revision Level	Date	Revision Description
1.0	June 1, 2000	Released for public review and comment
1.1	August 1, 2000	a) Modified RXERR and TXERR coding to reduce transitions and power in normal conditions. b) Removed CRS_COL pin and incorporated coding alternative for half duplex implementation. c) Found and corrected some inconsistencies in which clock was specified for timing. PHY generated signals are based on RXC and MAC generated signals are based on TXC. Specified that RXC is derived from TXC to eliminate need for FIFOs in the MAC. d) Modified timing diagram to incorporate PC board load conditions. e) Removed references to SMII due to broad concerns about IP exclusivity and added specification for 10/100 MII operation. f) Modified Intellectual Property statement to address incorporation of IP from multiple sources. g) Modified document formatting.
1.2	Sept 11, 2000	a) Changed TD[4]/TXEN_TXERR signal name to TX_CTL b) Changed RD[4]/RXEN_RXERR signal name to RX_CTL c) Removed 100ps jitter requirement from TXC d) Changed RXC derivation to received data stream e) Clarified Table 1 description of TX_CTL and RX_CTL logical functions f) Required CRS assertion/deassertion to be synchronous for all speeds. g) Returned timing numbers to absolute from percentages. h) Relaxed 10/100 Duty cycle requirements to 40/60 i) Added verbage to allow clock cycle stretching during speed changes and receive data and clock acquistion. j) Modified Table 4 to incorporate optional in-band signaling of link status, speed, and duplex. k) Slight wording change on IP statements to limit scope and indemnify.
1.2a	Sept 22, 2000	a) Clarified 3.4.2 statement to eliminate suggestion that in-band status was only required for half-duplex. b) Modified Table 2 to from "Clock to Data skew" to "Data to Clock skew" to clarify the fact that clock is delayed relative to data. c) Modified section 4.0 to clarify that MDIO/MDC are also operating at 2.5v CMOS levels.
1.3	Dec 10, 2000	a) Clarified RX_CTL and TX_CTL functionality by modifying Figure 4 and adding Figure 5 and Figure 6. b) Modified Table 3 to include the value of FF as reserved when TX_CTL=0,1. c) Reduced TskewR in Table 2 to a value of 2.6ns maximum for Gigabit operation and relaxed it in note #1 for 10/100 operation. d) Put maximum delay in note #1 of Table 2 of 2ns to ensure minimum setup time for subsequent edges.
2.0	April 1, 2002	a) Changed I/O specification to HSTL Class 1 per JESD 8-6 and removed table 5. b) Changed timing specification to allow transmitter to integrate delay previously allocated to PC layout and modified table 2.

1.0 Purpose

The RGMII is intended to be an alternative to the IEEE802.3u MII, the IEEE802.3z GMII and the TBI. The principle objective is to reduce the number of pins required to interconnect the MAC and the PHY from a maximum of 28 pins (TBI) to 12 pins in a cost effective and technology independent manner. In order to accomplish this objective, the data paths and all associated control signals will be reduced and control signals will be multiplexed together and both edges of the clock will be used. For Gigabit operation, the clocks will operate at 125MHz, and for 10/100 operation, the clocks will operate at 2.5MHz or 25MHz respectively.

2.0 System Diagram

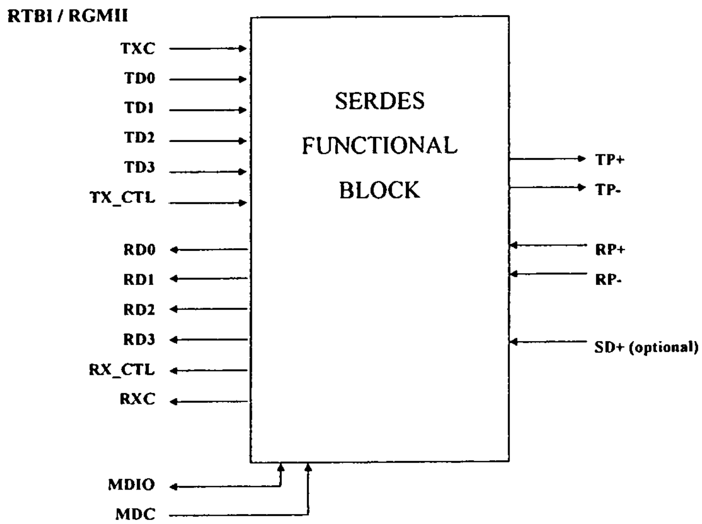

FIGURE 1 (System Diagram)

3.0 Signal Definitions

The RGMII will share four data path signals with the Reduced Ten Bit Interface (RTBI) and share control functionality with the fifth data signal. With the inclusion of the MDIO/MDC serial management signals, the RTBI will not require independent control signals like LK_REF, BYTE_EN, etc. Register assignment of SERDES control bits is left to the implementer.

Signal Name	RTBI	RGMII	Description
TXC	MAC	MAC	The transmit reference clock will be 125Mhz, 25Mhz, or 2.5Mhz +- 50ppm depending on speed.
TD[3:0]	PCS	MAC	In RTBI mode, contains bits 3:0 on ↑ of TXC and bits 8:5 on ↓ of TXC. In RGMII mode, bits 3:0 on ↑ of TXC, bits7:4 on ↓ of TXC
TX_CTL	PCS	MAC	In RTBI mode, contains the fifth bit on ↑ of TXC and tenth bit on ↓ of TXC. In RGMII mode, TXEN on ↑ of TXC, and a logical derivative of TXEN and TXERR on ↓ of TXC as described in section 3.4
RXC	PHY	PHY	The continuous receive reference clock will be 125Mhz, 25Mhz, or 2.5Mhz +- 50ppm. and shall be derived from the received data stream
RD[3:0]	PHY	PHY	In RTBI mode, contains bits 3:0 on ↑ of RXC and bits 8:5 on ↓ of RXC. In RGMII mode, bits 3:0 on ↑ of RXC, bits7:4 on ↓ of RXC
RX_CTL	PHY	PHY	In RTBI mode, contains the fifth bit on ↑ of RXC and tenth bit on ↓ of RXC. In RGMII mode, RXDV on ↑ of RXC, and a derivative of RXDV and RXERR on ↓ of RXC as described in section 3.4

TABLE 1 (Signal Definitions)

3.1 Signal Logic Conventions

All signals shall be conveyed with positive logic except as specified differently. For descriptive purposes, a signal shall be at a logic "high" when it is at a valid voltage level greater than V_{OH_MIN}, and logic "low" when it is at a valid voltage level less than V_{OL_MAX}.

3.2 Multiplexing of Data and Control

Multiplexing of data and control information is done by taking advantage of both edges of the reference clocks and sending the lower 4 bits on the ↑ edge and the upper 4 bits on the ↓ edge. Control signals can be multiplexed into a single clock cycle using the same technique.

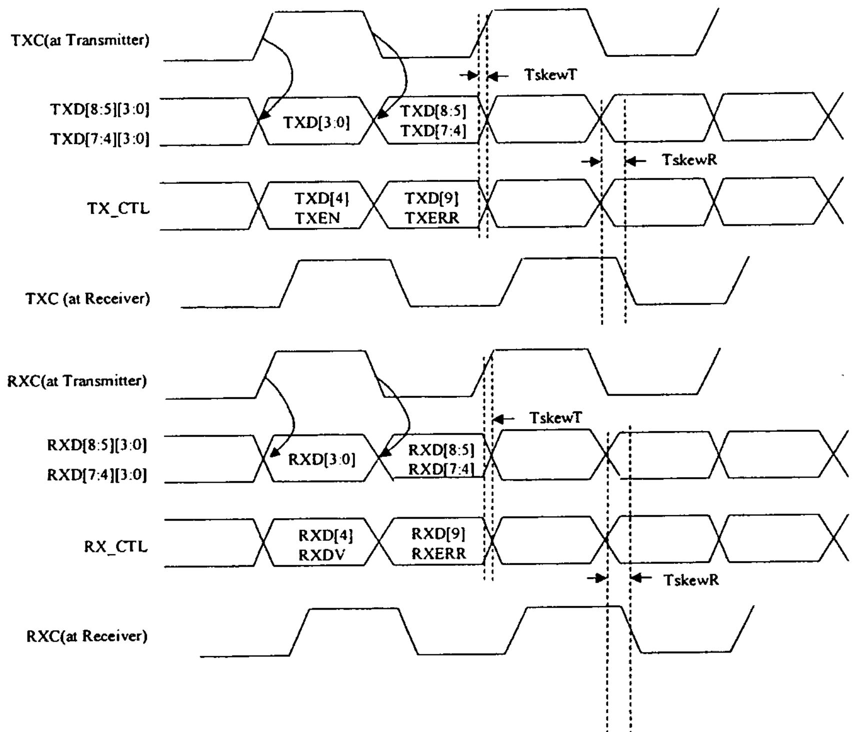

FIGURE 2 (Multiplexing & Timing Diagram)

3.3 Timing Specifics (Measured as defined in EIA/JESD 8-6 1995 with a timing threshold voltage of VDDQ/2)

Timing for this interface will be such that the clock and data are generated simultaneously by the source of the signals and therefore skew between the clock and data is critical to proper operation. This approach is being used to provide tighter control of skew. Timing values are defined in percentages of the nominal clock period so to make this table speed independent.

Symbol	Parameter	Min	Typical	Max	Units
TskewT	Data to Clock output Skew (at Transmitter)	-500	0	500	ps
TskewT1	Data to Clock output Skew (at Transmitter – integrated delay) *note 4	1.2	1.8	2.4	ns
TskewR	Data to Clock input Skew (at Receiver) *note 1	1	1.8	2.6	ns
Tcyc	Clock Cycle Duration *note 2	7.2	8	8.8	ns
Duty_G	Duty Cycle for Gigabit *note 3	45	50	55	%
Duty_T	Duty Cycle for 10/100T *note 3	40	50	60	%
Tr / Tf	Rise / Fall Time (20-80%)			.75	ns

note 1: This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns and less than 2.0ns will be added to the associated clock signal. For 10/100 the Max value is unspecified.
note 2: For 10Mbps and 100Mbps, Tcyc will scale to 400ns+-40ns and 40ns+-4ns respectively.
note 3: Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.
Note 4: TskewT1 allows implementation of a delay on TXC or RXC inside the transmitter. Devices which implement internal delay shall be referred to as RGMII-ID. Devices may offer an option to operate with/without internal delay and still remain compliant with this spec.

TABLE 2

3.4 TXERR and RXERR Coding

To reduce power of this interface, TXERR and RXERR, will be encoded in a manner that minimizes transitions during normal network operation. This is done by the following encoding method. Note that the value of GMII_TX_ER and GMII_TX_EN are valid at the rising edge of the clock while TXERR is presented on the falling edge of the clock. RXERR coding behaves in the same way.

TXERR <= GMII_TX_ER (XOR) GMII_TX_EN
RXERR <= GMII_RX_ER (XOR) GMII_RX_DV

When receiving a valid frame with no errors, RXDV=true is generated as a logic high on the ↑ edge of RXC and RXERR=false is generated as a logic high the ↓ edge of RXC. When no frame is being received, RXDV=false is generated as a logic low on the ↑ edge of RXC and RXERR=false is generated as a logic low on the ↓ edge of RXC.

When receiving a valid frame with errors, RXDV=true is generated as logic high on the ↑ edge of RXC and RXERR=true is generated as a logic low on the ↓ edge of RXC.

TXERR is treated in a similar manner. During normal frame transmission, the signal stays at a logic high for both edges of TXC and during the period between frames where no errors are to be indicated, the signal stays low for both edges.

TX_CTL	GMII_TX_EN	GMII_TX_ER	TXD[7:0]	Description	PLS_DATA.request parameter
0,0	0	0	00 through FF	Normal inter-frame	TRANSMIT_COMPLETE
0,1	0	1	00 through 0E	Reserved —	
0,1	0	1	0F	Carrier Extend	EXTEND (eight bits)
0,1	0	1	10 through 1E	Reserved —	
0,1	0	1	1F	Carrier Extend Error	EXTEND_ERROR (eight bits)
0,1	0	1	20 through FF	Reserved —	
1,1	1	0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1,0	1	1	00 through FF	Transmit error propagation	No applicable parameter

NOTE—Values in TXD[7:0] column are in hexadecimal

TABLE 3 (Allowable Encoding of TXD, TXERR and TXEN)

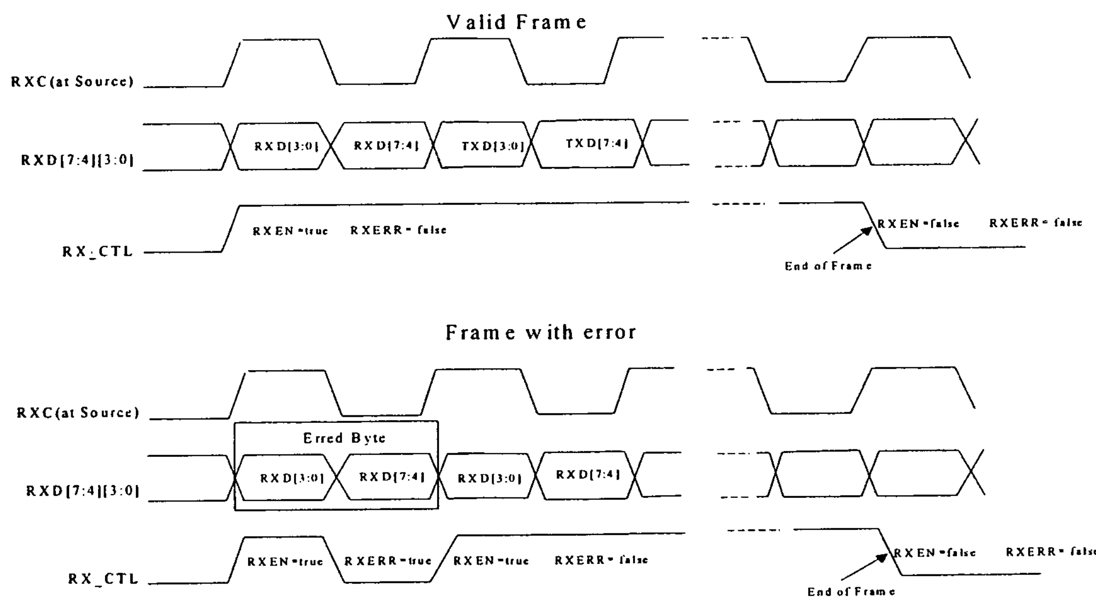

FIGURE 4

RX_CTL	GMII_RX_DV	GMII_RX_ER		RXD[7:0]	Description	PLS_DATA.indicate or PHY_ status parameter
0,0	0	0	#	xxx1 or xxx0	Normal inter-frame	Indicates link status 0=down, 1=up
0,0	0	0	#	x00x or x01x x10x or x11x	Normal inter-frame	Indicates RXC clock speed 00=2.5Mhz, 01=25Mhz, and 10=125Mhz, 11=reserved
0,0	0	0	#	1xxx or 0xxx	Normal inter-frame	Indicates duplex status 0=half-duplex, 1=full duplex
0,1	0	1	*	00	Reserved	—
0,1	0	1	*	01through 0D	Reserved	—
0,1	0	1	*	0E	False Carrier indication	False Carrier Present
0,1	0	1	*	0F	Carrier Extend	EXTEND (eight bits)
0,1	0	1	*	10 through 1E	Reserved	—
0,1	0	1	*	1F	Carrier Extend Error	ZERO, ONE (eight bits)
0,1	0	1	*	20 through FE	Reserved	—
0,1	0	1	*	FF	Carrier Sense	PLS_Carrier.Indicate
1,1	1	0	*	00 through FF	Normal data reception	ZERO, ONE (eight bits)
1,0	1	1	*	00 through FF	Data reception error	ZERO, ONE(eight bits)

* NOTE— (Required Function) Values in RXD[7:0] column are in hexadecimal.
# NOTE— (Optional) Values in RXD[7:0] column are in binary; nibbles are repeated on ↑ edge and ↓ edge.

TABLE 4 (Allowable Encoding of RXD, RXDV and RXERR)

3.4.1 In-Band Status (Optional)

In order to ease detection of the link status, speed and duplex mode of the PHY, inter-frame signals will be placed onto the RXD[3:0] signals as indicated in table 4. The status of the PHY shall be indicated whenever Normal Data, Data Error, Carrier Extend, Carrier Sense, or False Carrier are not present. When link status is down, PHY speed and duplex are defined by the PHY's internal setting.

3.4.2 In-Band Status (Required)

CRS is indicated by the case where RXDV is true, or the case where RXDV is false, RXERR is true, and a value of FF exists on the RXD[7:0] bits simultaneously or in the case where a Carrier Extend, Carrier Extend Error or False Carrier are occurring as defined in Table 4. Carrier Extend and Carrier Extend Error are applicable to Gigabit speeds only.

Collision is determined at the MAC by the assertion of TXEN being true while either CRS or RXDV are true. The PHY will not assert CRS as a result of TXEN being true.

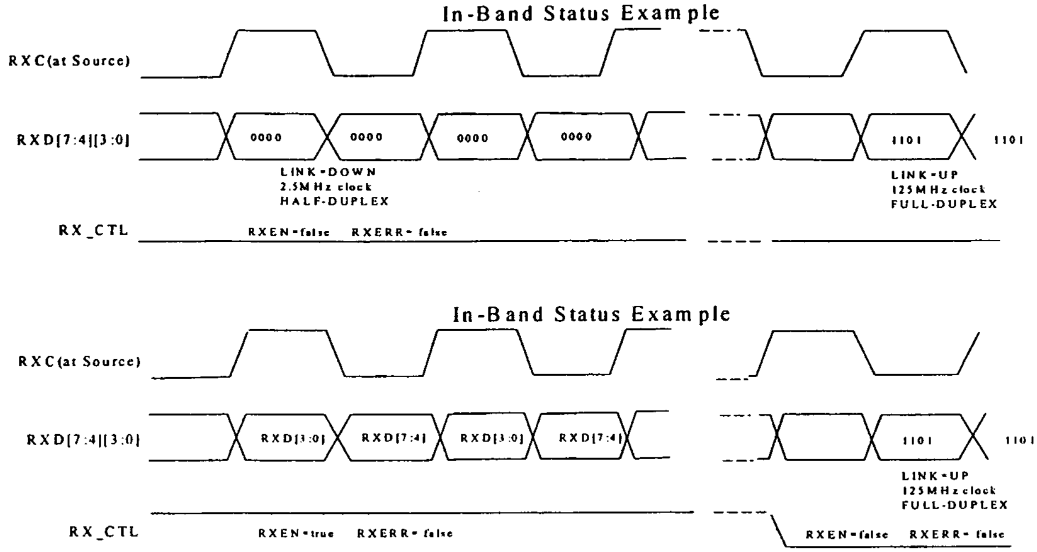

FIGURE 5

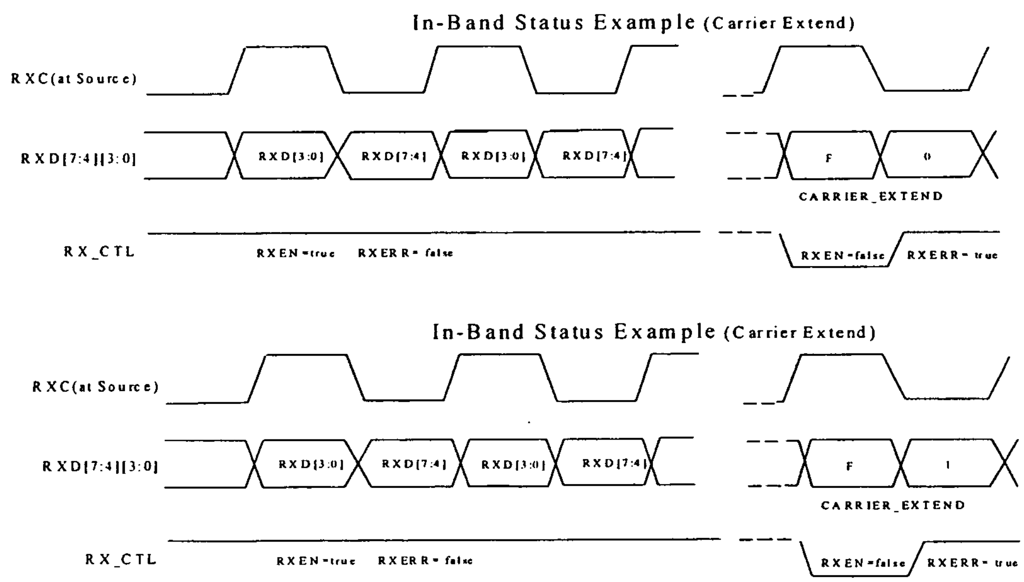

FIGURE 6

4.0 Electrical Characteristics

The RGMII and RTBI signals (including MDIO/MDC) will be based upon 1.5v HSTL interface voltages as defined by JEDEC EIA/JESD8-6. Please refer to that specification for details on the Class 1 drivers and receivers.

5.0 10/100 Functionality

This interface can be used to implement the 10/100 Mbps Ethernet Media Independent Interface (MII) by reducing the clock rate to 25MHz for 100Mbps operation and 2.5MHz for 10Mbps. The TXC will always be generated by the MAC and RXC will be generated by the PHY. During packet reception, the RXC may be stretched on either the positive or negative pulse to accommodate the transition from the free running clock to a data-synchronous clock domain. When the speed of the PHY changes, a similar stretching of the positive or negative pulses is allowed. No glitching of the clocks are allowed during speed transitions.

This interface will operate at 10 and 100Mbps speeds exactly the same way it does at Gigabit speed with the exception that the data may be duplicated on the ↓ edge of the appropriate clock.

The MAC will hold TX_CTL low until it has ensured that it is operating at the same speed as the PHY.

6.0 Mode Selection

The decision about which mode of operation this interface will use is left to the implementers. It may be done with hard-wired pins, or through register bits that are controlled by software.

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From: DOVE,DANIEL J (HP-Roseville,ex1) [IMCEAEX-_O=HP_OU=AMERICAS_CN=RECIPIENTS_CN=AM-31449@hardingmarketing.com]

Sent: Monday, June 10, 2002 1:48 PM

To: TAKATA,STAN (HP-Roseville,ex1)

Subject: RGMII spec onto ProCurve Website

Hi Stan,

We discussed putting these onto the website a week or so ago. I recommend putting them onto the FAQ site as it is a good spot for technical information.

http://www.hp.com/rnd/support/faqs/index.htm

I would like to propose the following verbage on the page that holds pointers to the two documents.

==

Reduced Gigabit Media Independent Interface (RGMII)

This interface was developed by Hewlett Packard with the objective of providing a low-cost, low-pin count interface for Gigabit Ethernet devices. Other companies have provided review and intellectual property in the development of this interface with the express intention of making it public domain.

RGMII version 1.3 was released in December of 2000 for implementation into .25u silicon. It required 2.5V CMOS I/O and PC board layout considerations to achieve proper timing. This was done for expediency and to ease silicon design criteria.

RGMII version 2.0 was released in April of 2002 for implementation into .18u and smaller geometry silicon. It uses HSTL class 1 I/O which reduces power and allows for compatibility with 2.5V CMOS designs. It also incorporates modified timing to allow direct connection between devices without PC board layout considerations for timing. It has been designed to allow accomodation of designs which use version 1.3 and 2.0 on the same PC board implementation as long as careful attention is paid to details. This version is recommended for all future designs that incorporate RGMII.

===

Please let me know when the documents hit the website and what the final URL is. I would like to send out an email to

Exhibit 15

the RGMII community letting them know where to find it.

Thanks,

Dan

Ticket # 18302 | Entered 6/10/2002 | Target 6/19/2002

Requested —— Submitted —— In Progress —— Approval —— Publication —— Closed

Project	Assignee	Entered By	Status	Priority
WndSite	marybeth_p	stan_t	closed	Medium

SUMMARY Please add the attached to http://www.hp.com/rnd/library/technology.htm

URL: (Live/Stage)
http://www.hp.com/rnd/library/technology.htm

Related URLs:
6/11/02, 2:00PM, stan_t - looks great, thanks! By the way, no need to add this to the FAQ's.

Additional Info. **Attachment** ☑

Attachment(s)
RGMII_spec_onto_ProCurve_Website.msg
RGMIIv1_3.pdf
RGMIIv2_0.pdf

Description
6/10/02, 5:02:24 PM - stan_t:
Please add the RGMII spec to the technology library.

Level of QA copy

Followups
6/11/02, 1:46:23 PM - mattg:
Page and PDF's released live.

6/11/02, 11:55:03 AM - marybeth_p:
Matt, OK to publish!

6/11/02, 11:06:04 AM - marybeth_p:
Stan, will this work?

6/11/02, 10:56:20 AM - mattg:
New section added and links made.

6/11/02, 9:46:54 AM - marybeth_p:
Matt, please add a new line in blue chiclet titled "reduced gigabit media independent interface (RGMII)" and link to a new section in table with the same name.

Please add 2 new lines in table: one with 1st 2 paragraphs from attached message, with link to attached RGMIIv1_3.pdf (-> pdf: 227 kb), second table line with 3rd paragraph of message, linked to attached RGMIIv2_0.pdf (-> pdf: 233 kb)

Exhibit 16